A METHODOLOGY FOR PHYSICAL MODELING OF HIGH-VOLTAGE/POWER INTEGRATED-CIRCUIT DEVICES FOR CIRCUIT SIMULATION

By

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. . . it is a tale told by an idiot,
full of sound and fury,
signifying nothing.

Shakespeare

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TABLE OF CONTENTS

ACKNOWLEDGEMENTS.....iii

ABSTRACT.....vi

CHAPTERS

1 INTRODUCTION.....1

2 A PHYSICAL MODEL FOR THE CONDUCTANCE OF LATERAL $p^{+}p\pi pn^{+}$ STRUCTURES FOR HVICs.....7

2.1 Introduction.....7
2.2 Model Development.....9
2.3 Physical Insight (Simplified Model).....20
2.4 Experimental Corroboration and Discussion.....27
2.5 Summary.....39

3 CHARGE-CONTROL ANALYSIS OF THE IGBT TURN-OFF TRANSIENT.....40

3.1 Introduction.....40
3.2 Model.....44
3.3 Discussion.....58

4 HIGH-VOLTAGE/POWER INTEGRATED-CIRCUIT DEVICE MODELING--A FIRST APPROACH.....64

4.1 Introduction.....64
4.2 Modeling Methodology.....67
4.3 SPICE Simulations and Discussion.....81
4.4 Summary.....95

5 HIGH-VOLTAGE/POWER INTEGRATED-CIRCUIT DEVICE MODELING.....97

5.1 Introduction.....97
5.2 Modeling Methodology.....100
5.3 Application/Demonstration.....109
5.4 Simulation/Verification.....121
5.5 Summary

6 SUMMARY AND CONCLUSIONS WITH RECOMMENDATIONS.....134

6.1 Summary and Conclusions.....134
6.2 Recommendations.....136

APPENDICES

A HIGH CURRENT CARRIER TRANSPORT IN WIDE-BASE BJTs.....139

B UDCS/SLICE/SPICE MODEL IMPLEMENTATION.....142

REFERENCES.....152

BIOGRAPHICAL SKETCH.....158

Abstract of Dissertation Presented to the Graduate School of the University of Florida in Partial Fulfillment of the Requirements for the Degree of Doctor of Philosophy

A METHODOLOGY FOR PHYSICAL MODELING OF HIGH-VOLTAGE/POWER INTEGRATED-CIRCUIT DEVICES FOR CIRCUIT SIMULATION

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This dissertation presents a modeling methodology for the construction of physical network representations for high-voltage/power integrated-circuit (HV/P IC) devices. The effects of multidimensional carrier flow, base-region conductivity modulation, significant emitter recombination, nonreciprocal transcapacitance, and the onset of latch-up (static and dynamic), heretofore unaccounted for in empirical circuit models, are physically accounted for in our charge-based formalism. The methodology is applied to

a representative HV/P IC device, the LIGBT, and the derived model is implemented in SPICE via user-defined controlled sources (UDCSs).

The methodology is supported by rigorous theoretical analyses of several HV/P IC devices, two-dimensional numerical device simulations with PISCES, and experimental results obtained from specially fabricated test structures. The resulting physical network representations, in addition to the CAD ability they afford, will facilitate optimal device (process) design under an actual circuit (transient) environment, a capability that most device simulators do not have.

CHAPTER 1
INTRODUCTION

The field of high-voltage and power integrated circuits is a rapidly emerging and expanding technology. Three basic processing efforts have made high-voltage/power (HV/P) devices practical for circuit integration: one, the advent of a lateral, double-diffused MOS (DMOS) process [De86], which produced integrated high-speed, high-voltage display drivers; two, improved isolation techniques, such as dielectric isolation [Be85, Sh80] and field reduction techniques such as RESURF [Ap79], which reduced parasitic interactions and provided higher breakdown voltages; three, the functional integration of bipolar and MOS devices [Ru83], which dramatically lowered device on-resistance and consequently increased the power handling capability of HV/P integrated circuits (ICs), while maintaining the advantages of the MOS gate. However, although great strides in the process technology of HV/P ICs have taken place, the area of circuit modeling for computer-aided-design (CAD) of HV/P ICs, especially for

those ICs employing MOS-controlled bipolar devices, has been at a near standstill. Common high-injection effects, such as conductivity modulation and enhanced back injection, are not properly accounted for in existing, empirical circuit models for HV/P devices [Pa86]. Furthermore, these models vitually ignore multidimensional carrier flow, which is typical in integrated HV/P devices. Thus, there exists a need for developing new physically based models for HV/P devices and implementing these models in a circuit simulator, e.g., SPICE [Na75].

This dissertation is concerned with the development and implementation of network representations for a general class of merged MOS-controlled bipolar structures, e.g., the lateral insulated-gate bipolar transistor (LIGBT) [Da84, Si85]. The major contributions made in this work are as follows:

(1) the general formulation and solution of the steady-state transport problem for the basic $p^+p_Bpn^+$ structure, in terms of quasi-Fermi level potentials, explicitly showing the effect of the p punch-through shield on the transport problem;

(2) the physical (charge-control) characterization of the IGBT turn-off transient, clearly identifying the device parameters controlling the important charging mechanisms;

(3) the development and experimental verification of a physical (charge-based) methodology for modeling HV/P IC structures including the effects of multidimensional carrier flow, base-region conductivity modulation, and enhanced back injection;

(4) the implementation of the LIGBT model into SPICE through user-defined controlled sources (UDCSs) with implicit characterizations and numerical representations for transconductances and transcapacitances.

In Chapter 2, we develop analytic models for the steady-state forward current-voltage characteristic of a (p^+pnpn^+) gated-diode switch (GDS) [We82]. The models, which apply generally to gated bipolar switches, are based on a system of equations derived from basic pin-diode theory. They provide physical insight into GDS operation and suggest optimal design criteria to minimize the dc and incremental resistances at high currents. Measured data taken from a variety of GDS test structures are discussed in support of the models.

In Chapter 3, a quasi-static charge-control analysis of the unique transient turn-off characteristic of the IGBT [Be85] is developed. The analysis describes the transient behavior in terms of steady-on-state current components that flow in the constituent MOSFET and BJT in the basic

IGBT structure. The effects of the expanding depletion region at the cathode and of minority-carrier injection into the anode are properly accounted for. Consequently the physics underlying the turn-off time is clarified, and device design criteria for shortening it, without considerably degrading the on-state current conduction capability, are suggested.

In Chapter 4, a novel methodology for flexible SPICE implementation of physical models for HV/P devices, accounting for their unique characteristics, is presented and demonstrated. The implementation is achieved, without having to modify the simulator code, by utilizing UDCSs that reference a subroutine which defines, not necessarily in explicit form, the system of model equations. The simultaneous solution of the equations, which describes the integrated charges in the device and the quasi-static terminal currents in terms of the terminal voltages, is effected by the SPICE2 nodel analysis. The methodolgy is exemplified by modeling a particular high-voltage device, the IGBT, in which conductivity modulation and latch-up are accounted for. SPICE simulations of dc and transient characteritics of IGBT switching circuits are discussed and shown to be representative of measurements. The flexibility of the modeling methodolgy for HV/P IC CAD is demonstrated by simulating effects of both static and dymanic latch-up in the merged bipolar/MOS structure of the IGBT.

In Chapter 5, to enable CAD of power integrated circuits, new physical models for lateral HV/P devices, in particular LIGBT [Da84, Si85, Mu87] structures, are developed and implemented in SPICE. The models are charge-based, and, via regional partitioning, account for the unique features of HV/P devices unaccounted for in conventional equivalent-circuit models. The implementation of the models in the circuit simulator is flexible and allows these features (e.g., multidimensional carrier flow, conductivity modulation, latch-up, transcapacitance) to be simulated without having to sacrifice much physics through excessive empiricism. Device measurements of specially designed test structures, supplemented with two-dimensional numerical device simulations, support the modeling methodology and the model parameter extraction.

We summarize, in Chapter 6, the main conclusions and accomplishments of this dissertation. We also suggest ideas and avenues for future research.

In Appendix A, we briefly describe high-current carrier transport in wide-base transistor structures. The resulting simplified model predicts a fundamental difference for the high-current βs of pnp and npn transistors. The physical insight afforded by the simplified analysis will be useful for device engineers designing complementary IGBTs.

In Appendix B, we briefly overview a representative UDCS SLICE/SPICE implementation of a charge-based network representation for a wide-base, low-β pnp bipolar transistor, a key model in the methodology for modeling HV/P devices as dicussed in Chapter 5.

CHAPTER 2
A PHYSICAL MODEL FOR THE CONDUCTANCE OF LATERAL $p^+p\pi pn^+$ STRUCTURES FOR HVICs

2.1 Introduction

This chapter concerns the forward, steady-state current-voltage characteristics $I(V_A)$ of a $p^+p\pi pn^+$ structure, the GDS [We82,Ha81], used in HVICs. We develop an analytic model for $I(V_A)$ based on a one-dimensional regional representation of the device. The model yields physical descriptions of $R_{ON}(=\Delta V_A/\Delta I)$ and the dc resistance $R_{DC}(=V_A/I)$ at high operating currents where these resistances must be minimized to ensure efficient GDS operation [Sm82]. Such minimization is aided by the model, which clearly identifies the underlying physical mechanisms and the associated parameters.

The resulting model also has applications to other HV/P IC devices employing punch-through shields (aka buffer regions) for which the development of effective and efficient network models for circuit simulation is of primary interest. In addition, the proper modeling of the

anode and cathode recombination, when high-injection obtains in the low doped-base region, provides the impetus for developing a new BJT model as derived in Chapters 4 and 5 and highlighted in Appendix A.

The gated diode switch (GDS), illustrated in Figure 2-1, is a dielectrically isolated high-voltage integrated circuit silicon device used in monolithic crosspoint arrays applicable to telephone switching networks. The device is basically a PIN-diode with an n^+ gate in the i(π) region and p shields surrounding the p^+ anode and the n^+ cathode. The n^+ gate facilitates the turn-off of the switch, but does not affect the forward bias (ON) characteristics, which closely resemble those of a PIN-diode at high-current levels. The cathode shield prevents punch-through between the gate and the cathode in the off-state, and has been shown to limit the injection of electrons into the π region and hence increases the incremental on-resistence of the device [Sm82]. The "anode shield" facilitates a reliable contact to the anode, but does not provide any electrical benefit.

Our one-dimensional analytic model, which can be applied generally to gated bipolar switches, and hence has application to HV/P ICs, is based on a system of equations derived from previously developed PIN-diode theory [Ha52,He68,Fl57,Be79] for high-injection conditions. The equations are solved numerically to yield the desired $I(V_A)$

characteristic. The model is more useful as an engineering-design aid than is a direct numerical solution of the fundamental carrier transport equations [Sm82] because it is simpler and because it affords physical insight. The role of the cathode p-shield, as well as those of the n^+ cathode, the p^+ anode, and the π region, in defining $I(V_A)$ is clearly described by the model, thereby aiding optimal GDS design.

The physical insight provided is utilized to develop an even simpler model, valid for high currents at which R_{ON} and R_{DC} are of interest, that requires no recourse to numerical techniques. This model, although not as accurate as the other, is useful because it enables quick assessments of possible device design modifications not only for the GDS, but also, as shown in Appendix A, for the BJT portion of the LIGBT. The models are supported by measured data taken from a variety of GDS structures fabricated at Bell Laboratories (Reading).

2.2 Model Development

The structure of the GDS, fabricated in a "tub" of dielectrically isolated (DI) silicon, is illustrated in Figure 2-1. Because the (anode-cathode) length is typically much longer than the tub thickness, the one-dimensional $p^+p\pi pn^+$ model, also shown in Figure 2-1, for the GDS is representative of the basic operation of the

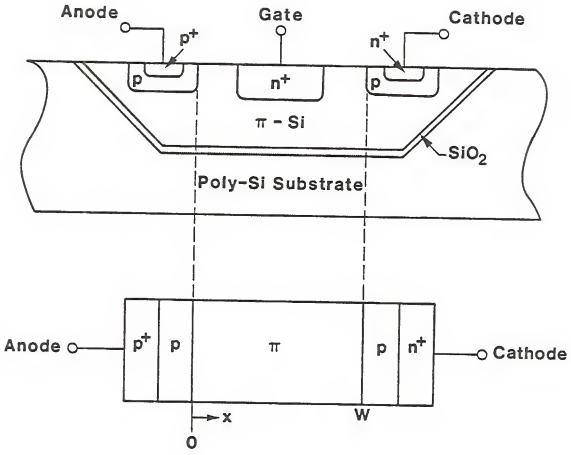

Figure 2-1. Gated-diode switch (GDS) cross section and corresponding one-dimensional model.

device. We are interested in the steady-state current-voltage characteristic of the GDS with the gate floating; the gate can therefore be ignored in the one-dimensional model.

In our development of the physical model, we use the quasi-Fermi levels to link the anode-cathode terminal conditions to the internal device physics. This approach facilitates physical insight into the operation of the device, especially with regard to how changes in excitation (carrier injection) at the cathode affect the excitation and recombination current at the anode. The energy-band diagram for a forward-biased GDS is shown in Figure 2-2. It implies how the applied anode-cathode voltage defines the hole and electron quasi-Fermi levels, E_{Fp} and E_{Fn}, and hence the carrier density and electric field in the device.

The applied voltage ($V_A>0$) equals the sum of the internal voltage drops:

$$V_A = V_J^{p^+p} + V_J^{p\pi} + V_\pi + V_J^{\pi p} + V_J^{pn^+} \qquad (2\text{-}1)$$

where $V_J^{p^+p}$ is the drop across the high-low junction in the anode, which is virtually zero because the p shield is doped high enough to prevent high-injection for all normal operating conditions; $V_J^{p\pi}$ is the drop across the p-π

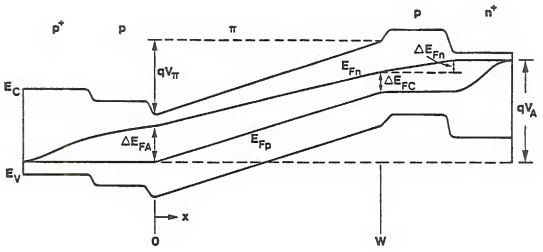

Figure 2-2. Energy-band diagram for a forward-biased GDS.

junction near the anode; V_π is the drop across the π region; $V_J^{\pi p}$ is the drop across the π-p junction near the cathode; and $V_J^{pn^+}$ is the drop across the p shield-cathode junction. Referring to Figure 2-2 and assuming high-injection ($p \simeq n >> N_{A\pi}$) where $N_{A\pi}$ is the acceptor doping density) in the π region, we have then from (2-1)

$$qV_A \simeq \frac{\Delta E_{FA}}{2} + \frac{\Delta E_{FC}}{2} + \Delta E_{Fn} + qV_\pi \qquad (2\text{-}2)$$

where ΔE_{FA} and ΔE_{FC} are the E_{Fn}-E_{Fp} separations at the p-π and π-p junctions respectively, and ΔE_{Fn} is the change in E_{Fn} across the p shield at the cathode. We assume that the majority-hole quasi-Fermi level is virtually flat across the p shield, in which the injection level is low; thus $qV_J^{pn^+} = \Delta E_{Fn} + \Delta E_{FC}$. In deriving (2-2) we used the quasi-equilibrium relations $qV_J^{p\pi} \simeq \Delta E_{FA}/2 - (kT)\ln(N_{A\pi}/n_i)$ and $qV_J^{\pi p} = \Delta E_{FC}/2 + (kT)\ln(N_{A\pi}/n_i)$.

Hence for a given GDS current density J, ΔE_{FA}, ΔE_{FC}, ΔE_{Fn}, and V_π must be determined before (2-2) can be used to give the desired $J(V_A)$ characteristic. These determinations are made by incorporating into basic PIN-diode theory a model for carrier transport in the p shield, which reduces the injection of electrons into the π region.

To account for the effect of the shield, i.e., to define ΔE_{Fn}, we neglect recombination in the shield, which is typically much less than the carrier fluxes through the shield. Then ΔE_{Fn} can be related to the electron current density J_N^S flowing in the shield, which constitues part of the total current density J described by basic PIN-diode theory.

For simplicity, we assume an (effective) uniformly doped shield. Since the shield-cathode junction is in low injection, the uniform-doping assumption implies that J_N^S is diffusion current, which is nearly constant:

$$J_N^S = qD_n\frac{\Delta n}{W_S} \cong \frac{qD_n n_i^2}{N_A W_S}\exp(\frac{\Delta E_{FC}}{kT})[\exp(\frac{\Delta E_{Fn}}{kT}) - 1] \qquad (2\text{-}3)$$

where D_n is the (average) electron diffusion coefficient in the shield, N_A is the (~ peak) doping density, and W_S is the (effective) width of the shield. From (2-3),

$$\Delta E_{Fn} \cong kT \ln\left[1 + J_N^S \frac{F_S \exp(-\frac{\Delta E_{FC}}{kT})}{kTn_i^2}\right] \qquad (2\text{-}4)$$

where

$$F_S \triangleq \frac{kTN_A W_S}{qD_n} \qquad (2\text{-}5)$$

is a shield factor that can be used to relate ΔE_{Fn} to the actual properties of the (diffused or implanted) p shield.

To relate F_S to an actual p shield in which N_A varies, note that generally

$$\Delta E_{Fn} \simeq \frac{kT}{q} J_N^S \int_{(\text{shield})} \frac{dx}{D_n(x)n(x)} , \qquad (2\text{-}6)$$

and that $n(x) \simeq 1/N_A(x)$. Since the greatest contribution to the integral in (2-6) comes from the region of the shield where $N_A(x)$ is a maximum (and $D_n(x)$ a minimum), F_S in (2-5) can be evaluated for this region, the width W_S of which can be estimated from the actual $N_A(x)$.

We now incorporate (2-4) into basic PIN-diode theory to characterize the conduction properties of the GDS. This involves generating a system of equations, the simultaneous solution of which for a specified J yields ΔE_{Fn}, ΔE_{FA}, ΔE_{FC}, V_π, V_A. The resulting $J(V_A)$ characteristic, with the cross-sectional area A (I=JA), then defines R_{DC} and R_{ON}. We note, based on results of calculations discussed in Section 2.4, that typically $\Delta E_{Fn} \sim kT$, which means that the shield reduces considerably the carrier injection level in the π region near the cathode and hence increases R_{DC} and R_{ON}.

The carrier transport (drift, diffusion, and recombination) in the π region is defined by the ambipolar transport equation [Ha52,He68]

$$\frac{d^2n}{dx^2} - \frac{n}{L_A^2} = 0 \qquad (2\text{-}7)$$

where

$$L_A \equiv 2\left[\frac{kT}{q}\left(\frac{\mu_n\mu_p}{\mu_n+\mu_p}\right)\tau_0\right]^{1/2} \quad . \qquad (2\text{-}8)$$

In writing (2-7), we have assumed, in addition to high injection (p≈n), that the electron and hole mobilities, μ_n and μ_n, are constant, and that the electron and hole (SHR) recombination times are equal (to τ_0) and constant. Effects of carrier-carrier scattering [Gh77] and band-band Auger recombination [Gh77], which tend to invalidate these assumptions, will be discussed later.

The high-injection assumption, which requires that τ_0 be long enough to avoid space-charge-limited flow [Ba70], is not restrictive with regard to modeling R_{DC} and R_{ON}. These resistances are defined for the GDS at relatively high values of J, which for typical values of τ_0 ensure high-injection levels. The boundary conditions for (2-7)

are thus simplified to

$$p(0) \simeq n(0) \simeq n_i \exp\left(\frac{\Delta E_{FA}}{2kT}\right) \qquad (2\text{-}9)$$

and

$$p(W) \simeq n(W) \simeq n_i \exp\left(\frac{\Delta E_{FC}}{2kT}\right) \qquad (2\text{-}10)$$

where x=0 and x=W denote the anode and cathode ends of the π region, the length of which is W (see Figure 2-1). The solution to (2-7) is then

$$p(x) \simeq n(x) \simeq \frac{n(0)\sinh\left(\frac{W-x}{L_A}\right) + n(W)\sinh\left(\frac{x}{L_A}\right)}{\sinh\left(\frac{W}{L_A}\right)}. \qquad (2\text{-}11)$$

This solution is coupled to the carrier transport in the anode and cathode by defining the minority-carrier recombination currents in those regions. In the p^+p anode, this current, which can be expressed as [Fo81]

$$J_N^A = J_{N0}\exp\left(\frac{\Delta E_{FA}}{kT}\right) \qquad (2\text{-}12)$$

is supported by electron injection from the π region:

$$J_N^A \simeq J_N(0) = \frac{b}{b+1} J + \frac{2kT\mu_n\mu_p}{\mu_n+\mu_p} \left.\frac{dn}{dx}\right|_{x=0} \qquad (2\text{-}13)$$

where $b\Delta\mu_n/\mu_p$. The expression for $J_N(0)$ in (2-13), which is evaluated using (2-11), derives [Fl57] from $J=J_N+J_p$ with p=n. In the n^+ cathode, the hole recombination current can be expressed as [Fo81]

$$J_P^C = J_{P0}\exp\left(\frac{\Delta E_{FC}+\Delta E_{Fn}}{kT}\right) \qquad (2\text{-}14)$$

and is supported by hole injection from the π region [Fl57]:

$$J_P^C \simeq J_p(W) = \frac{1}{b+1} J - \frac{2kT\mu_n\mu_p}{\mu_n+\mu_p} \left.\frac{dn}{dx}\right|_{x=W} . \qquad (2\text{-}15)$$

In (2-12) and (2-14), J_{N0} and J_{P0} are constant parameters (saturation current densities) that are defined by the properties of the heavily doped anode and cathode [Fo81].

Combining (2-4) with (2-12)-(2-15), we obtain the following system of three equations in the three unknowns, ΔE_{FA}, ΔE_{FC}, ΔE_{Fn}:

$$J_{N0}\exp(\frac{\Delta E_{FA}}{kT})=\frac{b}{b+1}J+\beta[\exp(\frac{\Delta E_{FC}}{2kT})-\exp(\frac{\Delta E_{FA}}{2kT})\cosh(\frac{W}{L_A})], \quad (2\text{-}16)$$

$$J_{P0}\exp(\frac{\Delta E_{FC}+\Delta E_{Fn}}{kT})=\frac{b}{b+1}j+\beta[\exp(\frac{\Delta E_{FC}}{2kT})-\exp(\frac{\Delta E_{FA}}{2kT})\cosh(\frac{W}{L_A})], \quad (2\text{-}17)$$

where

$$\Delta E_{Fn}=kT\ln\{1+[J\exp(\frac{-\Delta E_{FC}}{kT})-J_{P0}\exp(\frac{\Delta E_{Fn}}{kT})]\ \frac{F_S}{kTn_i^2}\} \quad (2\text{-}18)$$

$\beta=2kTn_i\mu_n\mu_p/L_A(\mu_n+\mu_p)\sinh(W/L_A)$. To solve the system, we must specify J_{P0}, J_{N0}, W, τ_0, and F_S. Then, for a given J, a suitable numerical method must be used to derive ΔE_{FA}, ΔE_{FC}, ΔE_{Fn}. We have used an IMSL subroutine to solve the system with a high degree of accuracy. From the solution n(x), J_N^A, and J_N^C are determined.

To generate the $J(V_A)$ characteristic, we must now determine V_π, which is the integral of the electric field across the π region. Again using basic PIN-diode theory [Ha52,He68], we have

$$V_\pi = \frac{J}{q(\mu_n+\mu_p)} \int_0^W \frac{dx}{n(x)} + \left(\frac{b-1}{b+1}\right) \frac{kT}{q} \ln\left[\frac{n(0)}{n(W)}\right]. \qquad (2\text{-}19)$$

The integration in (2-19) can be done analytically. Thus the combination of (2-19) with (2-9) and (2-10) defines, for a given J, V_π. Our characterization of $J(V_A)$ is then given by (2-1), (2-16)-(2-18), and (19), the solution of which must be obtained numerically. Representative results will be presented in Section 2.4.

2.3 Physical Insight (Simplified Model)

A numerical solution to the system of equations described in Section 2.2 is not necessary to gain useful physical insight into the GDS operation. In this section we describe this insight, and in doing so define a simpler analytic model for $J(V_A)$ that is valid for high values of J (100-1000 A/cm^2) of practical concern.

The total current J is the sum of the recombination currents in the p^+p anode, π, and n^+ cathode regions

[He68]:

$$J = J_N^A + J_\pi + J_p^C \quad . \tag{2-20}$$

From (2-9), (2-10), (2-12), and (2-14), we see that J_N^A and J_p^C are proportional to $[n(0)]^2$ and $[n(W)]^2$ respectively. In contrast, using (2-11) we see that

$$J_\pi = q\int_0^W \frac{n(x)}{2\tau_0}dx = \frac{qW\bar{n}}{2\tau_0} \tag{2-21}$$

where

$$\bar{n} \triangleq \frac{L_A}{W}\left\{\frac{\cosh(\frac{W}{L_A})-1}{\sinh(\frac{W}{L_A})}\right\}[n(0)+n(W)] \tag{2-22}$$

is an average carrier density in the π region. Thus as J increases, a larger portion of the current is supported by recombination in the anode and cathode regions; J_π becomes negligible. Furthermore, since $dn/dx \propto \bar{n}$, as can be seen by differentiating (2-11), the diffusion current in the π region becomes negligible as J increases [He68]; the holes and electrons predominantly drift across the π region.

Therefore for sufficiently high J, (2-13) and (2-15) can be simplified [He68] to

$$J_N^A \simeq \frac{b}{b+1} J \qquad (2\text{-}23)$$

and

$$J_P^C \simeq \frac{1}{b+1} J \quad . \qquad (2\text{-}24)$$

These simplifications can be easily checked for self-consistency with presumed high values of J using the model in Section 2.2. In fact it can be shown that for a given J, (2-23) and (2-24), with (2-12) and (2-14), yield valid approximations for ΔE_{FA} and $(\Delta E_{FC}+\Delta E_{FN})$ even when the diffusion current in the π region, reflected by the second terms in (13) and (15), is comparable to the drift current.

The approximation (2-24) enables an additional simplification regarding ΔE_{Fn} across the p shield. Combining (14), (18), and (24) yields

$$\Delta E_{Fn} \simeq \ln \left\{ \frac{1}{1 - \frac{bF_S J P0}{kTn_i^2}} \right\} \quad . \qquad (2\text{-}25)$$

Hence for sufficiently high J, ΔE_{Fn} is a constant, independent of J as well as W and parameters associated with the anode.

The approximations (2-23)-(2-25) are insightful. They imply that for a given high J, the injection level in the π region near the anode, i.e., n(0), is defined primarily by J_{N0}, and that the injection level near the cathode, i.e., n(W), is defined primarily by J_{P0} and F_S. This means that $V_J^{pn^+}$ is independent of W and the anode parameters, even though J_N^A is a significant component of J.

Consistent with the simplifications in (2-23)-(2-25) is the neglect of the second term in the expression (2-19) for V_π, which is typically ~kT/q. Thus for high J,

$$V_\pi \simeq \frac{J}{q(\mu_n+\mu_p)} \int_0^W \frac{dx}{n(x)} \qquad (2\text{-}26)$$

in which the integral is evaluated using (2-11). A further crude approximation can be made by writing (2-26) as

$$V_\pi \simeq \frac{JW}{q(\mu_n+\mu_p)\bar{n}} \qquad (2\text{-}27)$$

where $\bar{n}$ is given by (2-22). Although not as accurate as (2-26), (2-27) is insightful as we demonstrate later.

We have now defined a simpler analytic model for the high-current $J(V_A)$ characersitic of the GDS. For a given J, V_A is given by (2-2), in which V_π is approximated by (2-26) or (2-27), ΔE_{Fn} is approximated by (2-25), ΔE_{FC} is approximated by (2-14) and (2-24), and ΔE_{FA} is approximated by (2-12) and (2-23). We discuss the accuracy of this model in Section 2.4.

Using the insight accompanying the development of this model, we now offer a qualitative explanation of the complete current-voltage characteristic of the GDS. Typical measured characteristics are shown in Figure 2-3. The data were taken from a GDS test structure having two anodes placed at different lengths from the cathode. Figure 2-3 includes plots of $I(V_J^{pn^+})$ as well as $I(V_A)$ for both anodes. Note that the $I(V_J^{pn^+})$ characeristics are virtually coincident.

To explain the characeristics, we consider three distinct regions of the curves as indicated in Figure 2-3. Our models are applicable in region III where high-injection obtains in the π region. We note in this region that $I \propto \exp(qV_J^{pn^+}/kT)$ except for very high I where series resistance in the cathode ($\approx 3\Omega$) causes the characteristic to bend. Further, the $I(V_J^{pn^+})$ characteristics appears to be independent of W. These

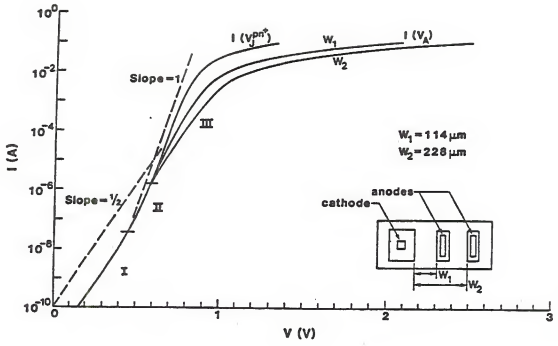

Figure 2-3. Measured GDS current versus applied voltage (V_A) and shield-cathod voltage drop (V_J^{pn}) for two different π-region lengths (W_1 and W_2). Three distinct regions (I,II,III) of operation are indicated.

observations are consistent with (2-14) and (2-24), which imply

$$J \simeq (b+1)J_{p0}\exp\left(\frac{qV_J^{pn^+}}{kT}\right) \qquad (2\text{-}28)$$

for high J.

The difference between the $I(V_J^{pn^+})$ and $I(V_A)$ curves in region III is

$$V_A - V_J^{pn^+} \simeq V_\pi \quad . \qquad (2\text{-}29)$$

The approximation (2-29) follows from (2-2) since $\Delta E_{FA} \simeq \Delta E_{FC}$, i.e., n(0)-n(W), for high J as discussed previously. The two $I(V_A)$ characteristics in Figure 2-3 are thus described in essence by (2-27), except for very high J where V_π is influenced by carrier-carrier scattering [Gh77] and band-band Auger recombination [Gh77]. Carrier-carrier scattering reduces the hole and electron mobilities, which tends to increase V_π as indicated in (2-27). Auger recombination reduces the carrier lifetime, which tends to decrease $\bar{n}$ in (2-22) and hence also increase V_π.

In the lower-current regions I and II in Figure 2-3, the $I(V_J^{pn^+})$ and $I(V_A)$ curves are coincident and are independent of W. In region I, $I \cong \exp(qV_A/2kT)$ is predominantly recombination in the shield-cathode junction space-charge region. Low injection prevails everywhere, and hence $V_A \cong V_J^{pn^+}$. For higher currents, but still low injection, in region II, J_π becomes important. However because $V_\pi \cong 0$, still $V_A \cong V_J^{pn^+}$ and $J_\pi \cong \exp(qV_A/2kT)$. The onset of high injection in the π region occurs near the transition point between regions II and III, where still $V_\pi << V_J^{pn^+} \cong V_A$. Above this point our model applies.

2.4 Experimental Corroboration and Discussion

In this section we present experimental data, taken from a variety of GDS structures fabricated at Bell Laboratories (Reading), that support the model described in Section 2.2. We also use the simpler analytic model developed in Section 2.3 to qualitatively explain the data. Finally we discuss model calculations that reveal the dependences of the current-voltage characteristic on critical device and material parameters.

Measured $I(V_J^{pn^+})$ and $I(V_A)$ in the high-injection regime are plotted in Figure 2-4. The data are taken from a GDS test structure having four anodes placed at different lengths from the cathode, two (W=228μm, 615μm) of which correspond to the data plotted. Also plotted in Figure 2-4

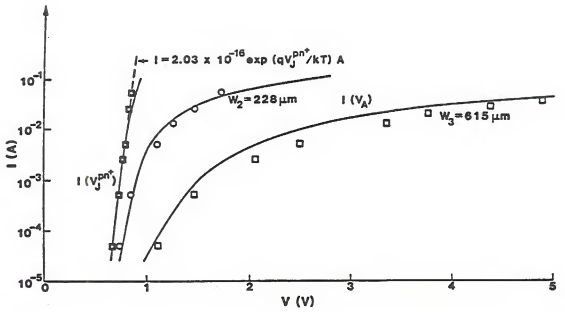

Figure 2-4. GDS current versus applied voltage (V_A) and shield-cathode voltage drop ($V_J^{pn^+}$) for two different π-region lengths (W_2 and W_3). The solid curves represent experimental measurements and the points represent calculations using the model derived in Section 2.2.

are the corresponding predictions yielded by the model in Section 2.2 through computer-aided numerical solution of the model equations.

The model parameter values used are listed in Table 2-1. They were initially estimated from knowledge of the device structure and of typical ranges of their values, using the insight afforded by the simpler model in Section 2.3, and then altered such that excellent correlation with the measured data was obtained. Hence the experimental-theoretical agreement not only supports the model, but also provides estimations of the important device and material parameters. We stress that these estimations are not a unique set; relatively small perturbations about these values do not significantly change the experimental-theoretical correlation.

The inferred value τ_0=10 μsec is not significantly influenced by band-band Auger recombination [Gh77] because $\bar{n} \lesssim 10^{17} cm^{-3}$, as implied by the calculations. However, the values μ_n=920cm^2/V-sec and μ_p=330cm^2/V-sec are in effect average values that reflect significant carrier-carrier scattering [Gh77] at the higher currents, an effect that we have not explicitly accounted for. This effect could be incorporated into the model if more exact parameter determinations were desired, but no additional insight into the operation of the GDS would be gained [Ch70].

The area $A=5X10^{-5}cm^2$ of the one-dimensional is merely an effective representation of the actual three-dimensional geometry. It is reasonable because it is comparable to the actual cathode and anode areas. The anode area is actually larger than the cathode area, which implies that J_{N0} and J_{F0} are perhaps more comparable in value than shown in Table 2-1.

We now discuss measured and predicted resistances of the GDS. The dc resistance, $R_{DC}=V_A/I$ at I=25mA, is plotted versus W^2 in Figure 2-5. The fact that both the experimental and theoretical plots become linear for long W supports in essence our model. This dependence is explained as follows. From (2-2) and (2-27),

$$R_{DC} \simeq \frac{W}{qA(\mu_n+\mu_p)\bar{n}} + \frac{1}{qI}\left(\frac{\Delta E_{FA}}{2} + \frac{\Delta E_{FC}}{2} + \Delta E_{Fn}\right) \quad (2\text{-}30)$$

where I=25mA. We note the actual R_{DC} differs from (2-30) by a constant series resistance, $(R_S^C+R_S^A)$, associated with the anode and cathode. Using (2-22), we see that for $W>3L_A$,

$$R_{DC} \simeq \frac{W^2}{qA(\mu_n+\mu_p)L_A[n(0)+n(W)]} + \frac{1}{qI}\left(\frac{\Delta E_{FA}}{2} + \frac{\Delta E_{FC}}{2} + \Delta E_{Fn}\right) \quad (2\text{-}31)$$

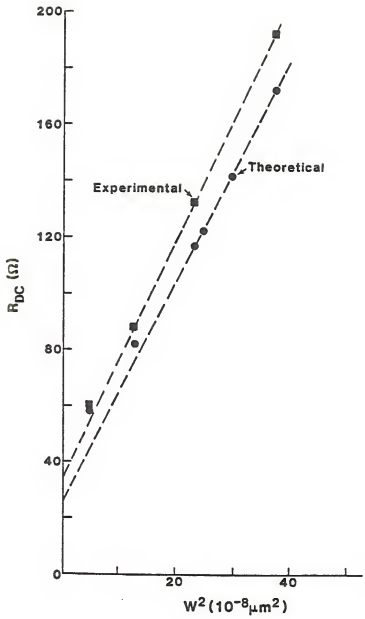

Figure 2-5. Measured and calculated dc resistance versus the square of the π-region length. The dashed lines emphasize the linear dependences.

and that for $W<0.3L_A$, the first term in (2-30) is linear in W, independent of L_A. We note, based on the discussion in Section 2.3, that the second term in (2-31), as well as n(0) and n(W), is virtually independent of W. Thus (2-31) correlates well with the plots in Figure 2-5. Discrepancies between the two slopes, i.e., in the slopes and in the extrapolated intercepts, can thus be attributed to the uncertainties in A, μ_n and μ_p (carrier-carrier scattering), and to the neglect of $(R_S^C+R_S^A)$ respectively.

Measured and predicted values of the incremental (quasi-static) resistance, $R_{ON}=\Delta V_A/\Delta I$ centered at I=30mA, are plotted versus W^2 in Figure 2-6. Referring to (2), we can write

$$R_{ON} \simeq \frac{\Delta V_\pi}{\Delta I} \qquad (2\text{-}32)$$

since the quasi-Fermi level terms vary little relative to ΔV_π at high currents. Differentiating (27) then, in which we note based on Section 2.3 that $J=I/A\simeq\bar{n}^2$ and that for $W>3L_A$, $\bar{n}\simeq(L_A/W)[n(0)+n(W)]$, we obtain

$$R_{ON} \simeq \frac{W^2}{qA(\mu_n+\mu_p)L_A[n(0)+n(W)]} , \qquad (2\text{-}33)$$

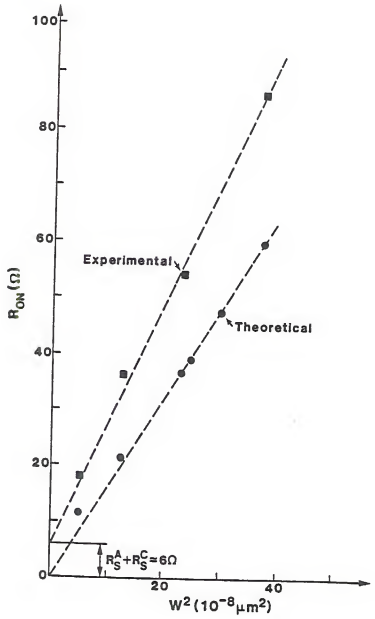

Figure 2-6. Measured and calculated incremental ON-resistance versus the square of the n-region length. The dashed lines emphasize the linear dependences. The determination of the extrinsic series resistance from the extrapolation of the experimental data is illustrated.

which corresponds well to the plots in Figure 2-6. $W<0.3L_A$, $\bar{n}=[n(0)+n(W)]/2$ and

$$R_{ON} \simeq \frac{W}{qA(\mu_n+\mu_p)[n(0)+n(W)]} \quad . \qquad (2\text{-}34)$$

As additional support for our theory, we note that (2-31) and (2-33) imply a factor of two difference between the slopes of the R_{DC} vs. W^2 and R_{ON} vs. W^2 characteristics, which is reflected by the measured data. We note further, since (2-33) does not account for $(R_S^C+R_S^A)$, that the extrapolation of the measured R_{ON} vs. W^2 characteristic yields directly this series resistance. We find $(R_S^C+R_S^A)\simeq 6\Omega$, which is about twice the value of R_S^C inferred from the measured $I(V_J^{pn^+})$ characteristic. Since we expect $R_S^A \simeq R_S^C$, this result provides additional support for our model. The significant discrepancy between the experimental and theoretical values of R_{ON} plotted in Figure 2-6 is due to, as we show later, our omission of an explicit accounting of the reduction in mobility caused by carrier-carrier scattering.

GDS design criteria to minimize R_{DC} and R_{ON} are suggested by (2-31), (2-33), and (2-34). From (2-9), (2-12), and (2-23),

$$n(0) \simeq n_i \left[\frac{bI}{A(b+1)J_{N0}} \right]^{1/2} , \qquad (2\text{-}35)$$

and from (2-10), (2-14), and (2-24),

$$n(W) \simeq n_i \left\{ \frac{I}{A(b+1)J_{P0}\exp(\frac{\Delta E_{Fn}}{kT})} \right\}^{1/2} \qquad (2\text{-}36)$$

where ΔE_{Fn} is constant as given by (2-25). Thus, reduction in both J_{N0} and J_{P0} would reduce R_{DC} and R_{ON}, but because a reduction in J_{P0} will also decrease ΔE_{Fn}, this will produce larger reductions in the resistances than a reduction in J_{N0}. We note from (2-25) also that designing the p shield such that $F_S \rightarrow 0$ would reduce the resistances, but would also tend to negate its shielding effect.

An increase in τ_0 will also decrease the resistances. For $W > 3L_A$, (2-31) and (2-33)-(2-36) show that R_{ON} and R_{DC} vary as $1/\tau_0^{1/2}$. However, for long τ_0, or short W ($W < 0.3L_A$), R_{ON} and R_{DC} are independent of τ_0; further decreases in W produce no additional reduction in the resistances. Because of the effects of carrier-carrier scattering, changes in parameters that increase n(0) and n(W), which tend to decrease the resistances, will also cause a reduction in carrier mobility, and hence the decreases in R_{ON} and R_{DC} predicted by (2-31) and (2-33) can be overestimated.

To demonstrate in more detail the influences of J_{N0}, J_{P0}, and τ_0 on he GDS resistance, we give in Table 2-2 calculated (using the model in Section 2.2) values of R_{DC} (I=25mA) and R_{ON} (I=30mA) for various values of these parameters. We chose an intermediate value for W=357μm, and we used the remaining parameter values in Table 2-1. The cathode and the anode series resistances were not included. We see from Table 2-2 that the resistances are most sensitive to J_{P0}, even though the "intrinsic" current-voltage characteristic, $J(V_J^{pn^+})$, can be independent of J_{P0} [see (2-28)]. Both R_{DC} and R_{ON} can be reduced considerably by increasing τ_0 and/or deceasing J_{N0} as well as J_{P0}.

The resistance values in parentheses in Table 2.2 were calculated by accounting for the carrier-carrier scattering using an iterative technique [Ch70]. That is, the carrier mobility values used in the final model calculation were chosen to be compatible with the calculated average carrier density in the π region as defined by empirical characterizations of the mobility-density dependences for holes and electrons. The calculations show that carrier-carrier scattering tends to diminish the reductions in resistance discussed above, especially with regard to R_{ON}. Nonetheless we can conclude, based on these calculations and others, that R_{ON} (intrinsic) for a typical

Table 2-1. GDS parameter values inferred from theoretical-experimental current-voltage correlation.

J_{N0}	=	$4X10^{-12}$	A/cm^2
J_{P0}	=	$1X10^{-12}$	A/cm^2
τ_0	=	$1X10^{-5}$	sec
F_S	=	$1.5X10^{11}$	$V\text{-}sec/cm^2$
μ_n	=	920	$cm^2/V\text{-}sec$
μ_p	=	330	$cm^2/V\text{-}sec$
A	=	$5X10^{-5}$	cm^2

Table 2-2. Calculated dependences of R_{DC} and R_{ON} on J_{N0}, J_{P0}, and τ_0 for W=357 μm. The remaining parameter values are given in Table 2-1. The values of R_{DC} and R_{ON} in parentheses were calculated accounting explicitly for carrier-carrier scattering [Ch70].

J_{N0} (A/cm^2)	J_{P0} (A/cm^2)	t_0 (μs)	R_{DC} (Ω)	R_{ON} (Ω)
$4X10^{-12}$	$1X10^{-12}$	10	81.7 (77.7)	21.5 (27.5)
$4X10^{-12}$	$5X10^{-13}$	10	69.4 (71.3)	16.1 (25.1)
$5X10^{-13}$	$1X10^{-12}$	10	62.3 (67.2)	12.5 (22.5)
$4X10^{-12}$	$1X10^{-12}$	50	68.5 (69.2)	16.5 (23.0)
$4X10^{-12}$	$5X10^{-13}$	50	59.6 (64.0)	12.4 (21.0)
$5X10^{-13}$	$1X10^{-12}$	50	54.2 (60.7)	9.6 (18.6)
$5X10^{-13}$	$5X10^{-13}$	50	50.2 (57.7)	7.7 (16.9)

GDS ($W \sim 200\mu m$, $A \sim 10^{-4} cm^{-2}$) can be reduced to $<10\Omega$ by decreasing J_{N0} and J_{P0} to $<10^{-12} A/cm^2$ and increasing τ_0 to $\sim 50\ \mu sec$.

2.5 Summary

A one-dimensional, regional model for the forward current-voltage characteristic of the GDS, as described in Section 2.1, has been presented and supported experimentally. It requires generally numerical evaluation of the analytic expressions, although for high currents it can be simplified to avoid the numerical characterization. The model yields expressions for the dc and incremental resistance of the GDS at high currents, which show for the GDS test structures used ($W > 3L_A$) that the R_{DC} and R_{ON} have W^2 dependence, that the slope of the R_{ON} vs. W^2 curve should be one-half of the slope of the R_{DC} vs. W^2 curve, and that the extrapolated intercept of the R_{ON} vs. W^2 curve should yield the series contact resistance ($R_S^C + R_S^A$). In addition to the familiar parametric dependences, the resistances were shown to decrease with increasing carrier lifetime in the π region and with decreasing saturation current desities for both the cathode and the anode.

CHAPTER 3
CHARGE-CONTROL ANALYSIS OF THE IGBT TURN-OFF TRANSIENT

3.1 Introduction

This chapter concerns the modeling of another common HV/P IC device, the IGBT [Ba85]. In Chapter 2, an analytical model for the steady-state I-V characteristics of a GDS was developed and experimentally verified. In this chapter we utilize the physical insight gained in modeling the GDS to develop a quasi-static charge control model for the IGBT turn-off transient [Ba85]. The model, with minor modifications, is also applicable to the hybrid IGBT (HIGBT) [Fo87,Si85] turn-off transient, as demonstrated in Chapter 5.

The analysis presented in this chapter describes the transient behavior of the IGBT in terms of its steady-state current components. The effects of minority-carrier injection into the anode are properly accounted for, within the limits of the quasi-static approximation, by using the physically correct PIN-diode boundary condition at the

anode. The resulting analysis identifies important charging mechanisms and suggests device design criteria for decreasing the turn-off time. The analysis subsequently aids in developing accurate and simple equivalent network representations for LIGBT structures, as shown in Chapters 4 and 5.

Until recently, high-voltage power-switching devices were either bipolar (e.g. gated PIN-diode [Sm82]) or MOS (e.g., power MOSFET [Ba81]). A particular application dictated the technology to be used based on a tradeoff between its advantages and disadvantages. Bipolar power devices generally yield low on-resistance R_{ON} (high-current-density operation) because of conductivity modulation, but slow switching because of the minority-carrier storage. MOS power devices are fast switching because of short minority-carrier (channel) transit time, but generally have high R_{ON} because of the lightly doped drift region.

Recently a new family of power semiconductor devices based on integrating bipolar and field-effect technologies was introduced. The IGBT [Ru83,Ba84b] is basically a MOSFET (VDMOS) having a pn junction connected to the drain that, in the on-state, injects minority carriers into, and modulates the conductivity of, the drain (drift) region. The basic IGBT structure is shown in Figure 3-1. With it, virtually any desired tradeoff between switching speed and

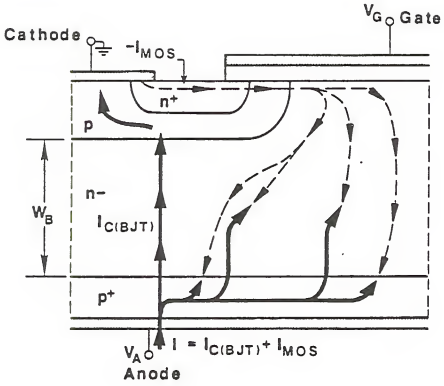

Figure 3-1. IGBT unit cell and current components. The solid arrows depict hole flow and the dashed arrows depict electron flow.

R_{ON} can be effected by controlling the carrier (recombination) lifetime in the n^- drift (epitaxial) region [Ba84a]. The device retains the high-input-impedance gate of the MOSFET, and has the added advantage of reverse-blocking capability.

The IGBT structure does, however, contain a parasitic pnpn thyristor that can latchup at high currents and thereby negate the gate control. Below the latchup current, the steady-state current-voltage characteristic (in the on-state) is defined by the DMOS, in series with the underlying (foward-biased) pn junction and in parallel with the parasitic vertical pnp bipolar-junction transistor (BJT). That is, the anode-cathode current comprises the DMOS channel current, which supplies electrons that recombine in accord with with the properties of the forward biased pn junction, and the BJT collector current, which results from holes injected from the underlying (emitter-base) junction.

The electrical coupling between the constituent MOSFET and BJT in the basic IGBT structure results in a unique transient turn-off characteristic [Ru83,Ba84b, Ba84a,Ba85,Ku85] comprising an initial rapid drop in forward current, followed by a slower decay. Previous analyses [Ru83,Ba84b,Ba84a,Ba85,Ku85] of this characteristic are either qualitative or incomplete, and do not adequately reflect the underlying physics to facilitate

optimal device design. In this chapter we develop a quasi-static charge-control (analytic) description of the transient turn-off characteristic, which is physically insightful and which suggests device design criteria for shortening the turn-off time, without increasing R_{ON} considerably.

The charge-control model we develop is similar to one previously developed Kuo et al. [Ku85], but does not involve the assumptions and approximations implicit in Kuo et al. [Ku85] that limit the validity of the model and in fact result in misconceptions concerning the physics underlying the turn-off transient. In particular, the effects of the expanding depletion region at the cathode and of minority-carrier injection into the anode, which are not currently accounted for in [Ku85], nor in earlier work [Ba84a], are represented in our model.

3.2 Model

The basic (unit-cell) structure of the (n-channel) IGBT, shown in Figure 3-1, comprises a DMOS FET merged with a BJT. The components of current, which is multidimensional, are indicated in the Figure 3-1 for the steady on-state (gate voltage V_G sufficiently positive to induce an n-channel between the the n^+ cathode an the n^- epi region, and the anode-cathode voltage $V_A>0$). The MOSFET channel (electron) current I_{MOS} supports carrier recombination in the BJT

$$I_{MOS} = I_{B(BJT)} \tag{3-1}$$

where $I_{B(BJT)}$ is the base current in the p^+n^-p BJT, which comprises recombination in both the base (n^- epi) and emitter (p^+ anode) regions. The IGBT (anode-cathode) current I is

$$I = I_{B(BJT)} + I_{C(BJT)} \tag{3-2}$$

where $I_{C(BJT)}$ is the collector current in the BJT, i.e., the base transport (hole) current. Note that the actual current gain of the BJT, $\beta = I_{C(BJT)}/I_{B(BJT)}$, depends critically on the geometry of the IGBT structure. Consequently, analysis of the device for the transient as well as steady-state conditions must somehow account for the multidimensional carrier flow.

The IGBT voltage V_A can be written as the sum of four voltage drops

$$V_A = V_J^{p^+n^-} + V_{epi} + IR_S + I_{MOS}(R_E + R_D) \tag{3-3}$$

where $V_J^{p^+n^-}$ is the drop across the underlying p^+n^- junction; V_{epi} is the vertical drop across the (conductivity-modulated) epi region; IR_S is the drop across the extrinsic series resistance R_S; and the last term is the (lateral) drop across the channel of the MOSFET, where, following [Su80], R_E and R_D represent effective lumped-channel resistances of the "series-connected" enhancement- and depletion-mode devices. The implicit formulation in terms of the junction voltages for the steady-state IGBT transport problem, and its corresponding numerical solution, are given in chapters 4 and 5.

The conductivity modulation that produces the excellent steady-state forward current-voltage characteristic, viz., low R_{ON}, of the IGBT can unfortunately cause the turn-off time to be much longer than that of a conventional power MOSFET. A typical IGBT turn-off transient [Ru83,Ba84b,Ba84a,Ba85,Ku85] is unique as illustrated in Figure 3-2. It shows an initial rapid drop in the forward current, followed by a slower decay, which reflects the lifetime of the carriers stored in the epi region. The turn-off time can be shortened by reducing the carrier lifetime, for example, via electron irradiation [Ba84a] or intentional metallic impurity doping [Go83]. Such techniques have resulted in turn-off times of less than 200ns, but with accompanying increases in R_{ON} because of the reduced carrier injection levels in the epi region.

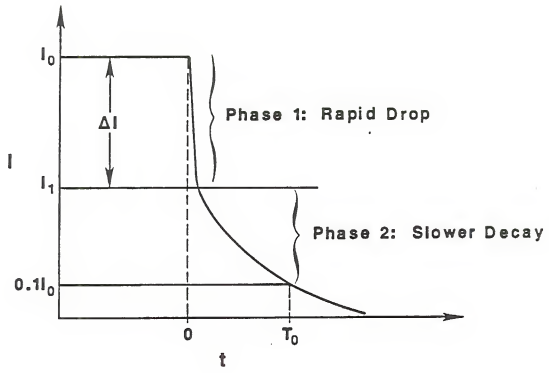

Figure 3-2. Typical IGBT turn-off transient showing two distinct phases.

The IGBT is turned off by removing the gate voltage, and hence the MOS channel through which electrons flow for recombination in the p^+ anode and n^- epi regions. The removal of the channel occurs quickly, on the order of the electron transit time which is typically a few tenths of a nanosecond [Ba81]. In order to characterize the IGBT turn-off transient, the external circuit, represented in Figure 3-3, must be considered. When the channel is removed (virtually instantaneously), $I_{MOS} \rightarrow 0$, but I cannot drop instantaneously because the reverse bias on the pn^- junction (J2 in Figure 3-3) does not increase abruptly; the depletion capacitance of J2 is (partially) charged in short but finite time, as controlled by the external circuit. This initial phase is completed when I, defined by the external circuit and developed reverse bias on J2 (V_{J2}), equals the time-dependent BJT collector current, defined by the (time-dependent) depletion-region width of J2. Little carrier recombination occurs during this fast transient. The second phase of the turn-off, however, is controlled by carrier recombination in the epi region (and perhaps in the anode region), and hence the completion of the development of V_{J2} is slower than the first phase. The carrier lifetimes are typically longer than the time constant that characterizes the initial transient.

Since the first phase is usually much faster than the second, we will characterize the composite turn-off by

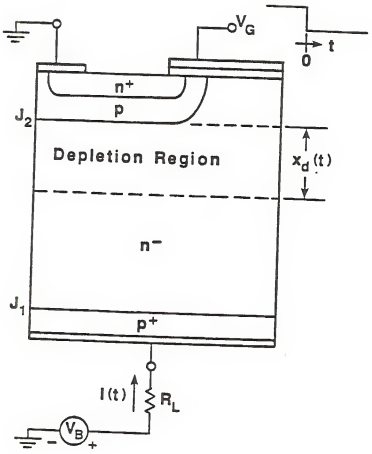

Figure 3-3. External biasing and turn-off circuitry for the IGBT transient analysis.

first describing only the fast drop ΔI in the current that occurs in the first phase, and then modeling the subsequent decay of I(t) in the second phase, which defines the turn-off time. If V_G is removed at t=0, and $I=I_0$ in the steady-state for t<0 as described by (3-2), then for t>0

$$I(t) \simeq I_{C(BJT)}(t) + \frac{dQ_{J2}(t)}{dt} \qquad (3-4)$$

where Q_{J2} is the charge associated with the depletion capacitance of J2. For $t=0^+$, I is I_0, and $I_{C(BJT)}$ and dQ_{J2}/dt, which equals I_{MOS} in (3-1), are defined by the steady-state characterization of the IGBT, $I(V_A)$. Hence our transient analysis is dependent on the steady-state model. We stress, however, the utility of the transient model, independent of the steady-state analysis. As we will show, the dc current components in (3-1) and (3-2) become parameters of the transient model and can evaluated by comparing theoretical and experimental characterizations of the turn-off transient.

Using a charge-control representation, we express the transient BJT collector current in (3-4) as

$$I_{C(BJT)} \simeq \frac{Q_p(t)}{\tau_{tp}(t)} \qquad (3-5)$$

where $Q_p(t)$ is the hole charge stored in the quasi-neutral n^- base region and τ_{tp} is base transit time for holes. The transit time in (3-5) is time-dependent because the depletion region (width x_d) of J2 is expanding. This moving boundary, which is not accounted for properly in previous work [Ba85,Ku85], is most important in the first phase of the as we demonstrate below. For prevalent high-injection conditions, we assume [Gh77]

$$\tau_{tp}(t) \simeq \frac{[W_B - x_d(t)]^2}{4K_A D_p} \qquad (3\text{-}6)$$

where W_B is the metallurgical base width of the vertical p^+n^-p BJT and K_A is a constant less than unity discussed below. Rigorously (3-6) (with $K_A=1$) applies to a one-dimensional device in which there is no recombination in the base nor back injection into the emitter. However, we assume that it (with $K_A<1$) is representative of the actual IGBT structure illustrated in Figure 3-1. Independent of the finite base current, K_A accounts for the multidimensional carrier flow in the epi, in which case to first order it could be given as the ratio of the BJT collector and emitter areas. We note also that $K_A \neq 1$ can effectively account for the influence of the base current (recombination in both the n^- epi and the p^+ anode) on the transit time [Ku85].

Because the carrier lifetime (in the base) is long relative to the duration of the initial fast transient, we assume that Q_p is invariant in the first phase, even though the holes (and electrons) are redistributed in time in the epi region. Thus as holes are swept out of the collector to increase Q_{J2}, electrons are forced toward the emitter, thereby increasing the hole injection from the emitter to maintain neutrality. This increase in Q_p, which approximately equals the increase in Q_{J2}, is much smaller than Q_p and hence does not threaten the validity of (3-5). From (3-1), (3-2), (3-5), and (3-6) then, we can write

$$I_0 \simeq I_{MOS} + \frac{Q_{p0}}{W_B^2/4K_AD_p} \qquad (3-7)$$

since $x_d \simeq 0$ for $t<0$. Equation (3-7) defines Q_{p0}, the steady-state value of Q_p, which remains virtually intact during the initial first transient.

The fast transient subsides when $dQ_{J2}/dt \to 0$, or from (3-4)-(3-7) when $I \to I_1$ where

$$I_0 = \frac{Q_{p0}}{(W_B-x_{dm})^2/4K_AD_p} \equiv \frac{I_0-I_{MOS}}{(1-x_{dm}/W_B)^2} . \qquad (3-8)$$

In (3-8), x_{dm} is the "final" value of x_d corresponding to the "final" reverse bias V_{J2m}, which for I_1 low enough that the hole density in the depletion region is indeed negligable, is [Gh77]

$$x_{dm} \simeq \left(\frac{2\varepsilon_S V_{J2m}}{qN_{epi}}\right)^{1/2} . \qquad (3\text{-}9)$$

The external circuit (Figure 3-3) in which R_L is chosen so that $I=I_0$ in the steady on state defines V_{J2m} (>0):

$$V_{J2m} \simeq V_B\left(1 - \frac{I_1}{I_0}\right). \qquad (3\text{-}10)$$

From (3-7) and (3-8) then,

$$\Delta I \triangleq I_0 - I_1 \simeq I_{MOS}\left\{1-\beta\left[\frac{1}{(1-x_{dm}/W_B)^2} - 1\right]\right\} \qquad (3\text{-}11)$$

where I_0, I_{MOS}, and β [$\equiv (I_0-I_{MOS}/I_{MOS}$] are described by the steady-state analysis. Note that $\Delta I<I_{MOS}$; viz., the fast drop in the current is, in general, less than the (steady-state) MOSFET current. Only for $x_{dm}<<W_B$ is $\Delta I \simeq$

I_{MOS}, which is wrongly implied in Baliga [Ba85] and Kuo et al. [Ku85].

To demonstrate the virtual independence of the transient result (3-11) from the steady-state analysis, which defines I_0 and I_{MOS}, we combine (3-9)-(3-11) to obtain

$$x_{dm} \simeq [\frac{2\varepsilon_S V_B}{qN_{epi}}(\frac{\Delta I}{I_0})]^{1/2} . \qquad (3\text{-}12)$$

Thus measurement of the first phase of the turn-off transient, i.e., of I_0 and ΔI, enables evaluation of x_{dm}, which from (3-11) describes the constitution (I_{MOS} and $I_{C(BJT)}$) of the steady-on-state current I_0.

The slower decay of I [from I_0-ΔI) to zero] in the second phase of the turn-off is similar to the transient response of a BJT in the active mode following the abrupt removal of the base current [Mu77]. Whereas the first-phase transient is controlled predominantly by the charging of the J2 depletion capacitance, we assume that the second-phase transient is controlled by carrier recombination. Thus the J2 displacement current [dQ_{J2}/dt in (3-4)] is neglected, and we write, based on (3-5),

$$I(t) \simeq \frac{Q_p(t)}{\bar{\tau}_{tp}} \qquad (3\text{-}13)$$

where $\bar{\tau}_{tp}$ is an average transit time, which can be crudely approximated based on (3-6), as

$$\bar{\tau}_{tp} \simeq \frac{(W_B - x_{dm})^2}{4K_A D_p} \qquad (3\text{-}14)$$

with x_{dm} given by (3-12). The use of (3-14) greatly simplifies the analysis of the second transient, and hence facilitates physical insight and identification of critical device parameters that define the turn-off. The simplication is representative because typically the increase in x_d beyond x_{dm} is less than x_{dm}; the relative change in τ_{tp} during the transient during the transient is smaller than that of Q_p. The decay of I(t) in our model is thus defined predominantly by the time-dependence of $Q_p(t)$ [Ku77]; and errors resulting from the use of (3-14) are minor and do not derogate the utility of the model.

In BJT terminology, I(t) is the emitter current, which is equated in (3-13) to the collector current because the base current is constrained to zero [Mu77]:

$$\frac{Q_p(t)}{\tau_H} + \frac{dQ_p(t)}{dt} + \frac{Q_n(t)}{\bar{\tau}_n} + \frac{dQ_n(t)}{dt} = 0. \qquad (3\text{-}15)$$

We are assuming that high injection (p=n) prevails in the base region throughout the main turn-off transient, and hence we use the high-injection carrier lifetime τ_H as defined by SRH theory [Gh77]. This is a reasonable assumption for a device in which conductivity modulation is essential in the on-state. In (3-15), Q_n is the minority electron charge in the quasi-neutral p^+ anode (emitter) region and $\bar{\tau}_n$ is an average (effective) electron lifetime (charge-control time). The dynamics of Q_n, which is not accounted for properly in previous work [Ba85,Ku85], can influence the second-phase transient as we show below.

For quasi equilibrium and negligible recombination in the p^+n^- junction space-charge region, Q_n can be related to Q_p using the quasi-static approximation. In the quasi-steady state, the solution [Gh77] to the ambipolar transport equation in the quasi-neutral base region (with p=n) yields, for (W_B-x_{dm}) less than the ambipolar diffusion length, $Q_p=qA(W_B-x_{dm})p(0)/2$ where p(0) is the hole density at the edge of the space-charge region and A is the device area. Using $Q_n/\bar{\tau}_n=AJ_{N0}[p(0)/n_i]^2$ [Gh77], where J_{N0} is the saturation current density associated with the electron injection (recombination) into the p^+ anode, we have

$$Q_n = \frac{Q_p^2}{Q_0} \qquad (3\text{-}16)$$

where Q_0 is a constant charge given approximately by

$$Q_0 \approx \frac{Aq^2 n_i^2 (W_B - x_{dm})^2}{4\bar{\tau}_n J_{N0}} \quad . \qquad (3\text{-}17)$$

With (3-16), (3-15) is a first-order, nonlinear differential equation for the quasi-static $Q_p(t)$, which can be solved analytically. If we assume $\bar{\tau}_n << \tau_H$, which is likely for the asymmetrically doped p^+n^- junction, we get

$$Q_p(t) \approx \frac{Q_{p0}\exp(-\frac{t}{\tau_H})}{1 + \frac{Q_{p0}\tau_H}{Q_0\bar{\tau}_n}[1-\exp(-\frac{t}{\tau_H})]} \qquad (3\text{-}18)$$

where t=0 is now taken as the start of this second-phase transient. Now I(t) is defined by (3-13), (3-14), and (3-18), which with (3-8) yield

$$I(t) \approx \frac{I_1\exp(-\frac{t}{\tau_H})}{1 + \frac{I_1 J_{N0}\tau_H}{AK_A q^2 n_i^2 D_p}[1-\exp(-\frac{t}{\tau_H})]} \quad . \qquad (3\text{-}19)$$

Thus I(t) can decay faster than exponentially if currents associated $Q_n(t)$, reflected by the second term in the denominator of (3-19), are significant. If J_{N0} is negligibly small, then (3-19) reduces to a simple exponential decay defined by the numerator. However for typical values of the model parameters, the second term in the denominator of (3-19) can be significant.

3.3 Discussion

Our analysis of the IGBT turn-off transient is first order, and describes, in terms of the steady-on-state current components, an initial fast drop ΔI of the current, followed by a slower decay of I(t), which can be, depending on J_{N0}, somewhat sharper than an exponential fall-off having a time constant equal to τ_H. In Figure 3-4 we plot the composite turn-off characteristic for a typical IGBT predicted by our analysis for three assumed values of τ_H and of J_{N0}, the two most significant material parameters that must be controlled for optimal device design. As noted previously, a steady-state analysis is needed to evaluate parameters in our transient model. In the derivation of the I(t) characteristics plotted in Figure 3-4, we first used a numerical solution of the steady-state ambipolar transport in a quasi-two-dimensional representation of the wide-base p^+n^-p BJT to estimate the constitution of I_0 in (3-1) and (3-2). Then, with I_{MOS} and

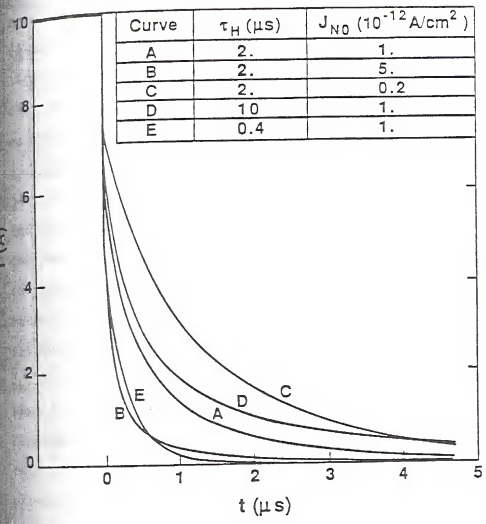

Figure 3-4. Calculated IGBT turn-off transient for three values of τ_H and of J_{N0}. Device parameter values used are $A = 0.1$ cm^2, $W_B = 60$ μm, $N_{epi} = 5 \times 10^{14}$ cm^{-3}, and $K_A = 0.5$; $I_0 = 10$ A.

β evaluated for a specified I_0, (3-9)-(3-11) give ΔI and (3-19) describes the transient decay I(t). The value of K_A (=0.5) used in the transient analysis is consistent with the quasi-two-dimensional treatment of the steady-state carrier transport: $K_A \simeq A_{collector}/A$.

Comparisons of the predicted characteristics in Figure 3-4 with published data [Ru83,Ba84b,Ba84a,Ba85,Ku85,Go83] indicate that our model is representative of typical IGBTs. The dependence on τ_H of both ΔI and I(t) is consistent with corresponding measurements. The dependence on J_{N0} has not been studied experimentally, but is, we believe, depicted faithfully. The predicted ΔI increases with increasing J_{N0}, for I_0 held constant, because β decreases. For the same reason, ΔI increases with increasing τ_H, but the dependence is not unrelated to the value of J_{N0}, and the change is not simply equal to I_{MOS} ($=I_0/\beta$) as implied in previous work [Ba85,Ku85].

The I(t) dependence also may be more complex than previously indicated [Ba84a,Ba85,Ku85]. Whereas the time dependence predicted for $J_{N0}=2X10^{-13}$ A/cm^2 is nearly exponential [$\tilde{\alpha}$ $\exp(-t/\tau_H)$], indicating that the second term in the denominator of (3-19) is unimportant, the predicted transients become supra-exponential as J_{N0} increases. This dependence of course is related to τ_H, becoming significant as τ_H decreases. For τ_H sufficiently short, and/or for J_{N0} sufficiently small, I(t) is exponential and T_0 is defined directly by τ_H.

The dependence of T_0 on carrier lifetime illustrated by the carrier lifetimes plotted in Figure 3-4 is consistent with other measurements [Ba84a,Ba85] that show T_0 decreasing strongly with increasing electron irradiation dose. Calculations and measurements imply $T_0 \tilde{\propto} \tau_H^{-1}$, which implies that the time dependence in the denominator of (3-19) is unimportant for these devices (that have low τ_H). We note further that measured dependences [Ba84a,Ba85] of T_0 on V_B and on I_0 are explained well by our first-order model. For a given τ_H, calculations show T_0 increasing weakly with increasing V_B for constant I_0, and decreasing with increasing I_0 for constant V_B. The $T_0(V_B)$ dependence is weak because x_{dm} in (3-12) and implicitly in (3-13), which defines T_0, does not change appreciably when I_0 is held constant, as can be seen from (3-10) and (3-11). The $T_0(I_0)$ dependence is more pronounced (T_0 can be halved by increasing I_0) because ΔI in (3-11) increases more rapidly than I_0; viz., I_{MOS}, which includes the p^+ anode recombination component, increases faster than I_0. We infer from the model however that T_0 will saturate for sufficiently high I_0 becauses ultimately I_{MOS}, which comprises predominantly the anode recombination current, becomes proportional to I_0.

From our analysis, we can suggest a way to quicken the turn-off, independent of shortening τ_H which increases R_{ON}

because V_{epi} in (3-3) increases. For a given τ_H, the turn-off time can be reduced by increasing ΔI, which decreases the second-phase decay in I(t) needed to turn off the device, and by enhancing the significance of the denominator in (3-19), which exploits the supra-exponential decay. Physically, these changes lower β and make I_{MOS}, which is controlled directly and without delay by the gate, a larger component of the steady-on-state current, and they make carrier removal through the p^+ anode more significant in the transient. They can be effected by increasing J_{N0}, which could be done perhaps by reducing the doping density and the electron lifetime and/or transit time in the heavily doped p^+anode region [Fo81]. The benefit of such an increase is illustrated in Figure 3-4. Reducing K_A in (3-19), for example by decreasing the BJT collector-emitter area ratio, would produce similar benefit. We note however from (3-3) that if the MOSFET resistances R_E and R_D are substantial, then increasing J_{N0} and/or decreasing K_A (i.e., reducing β) could significantly increase R_{ON}.

An n^+ punch-through shield (buffer region), as described in Chapter 2, may also be used in IGBT structures. The n^+ buffer region reduces the emitter efficiency of the constituent wide-base BJT and, for a given current level, makes I_{MOS} a larger component of the steady-on-state current, thus subsequently decreasing the turn-off time. The methodology for characterizing the

effects of a buffer region on device performance, as presented in Chapter 2, may be applied to IGBT structures to study the trade-off between decreased turn-off time and increased on-resistance arising from the buffer-induced reduction in base-region mobile carrier concentration.

The utility of the physical insight afforded by our model for the transient turn-off should be stressed. Whereas previous work has shown that T_0 is reduced by decreasing τ_H and increasing ΔI, it has not demonstrated how the reduction obtains and it has not clearly revealed how ΔI can be increased most effectively. Furthermore the previous work, which is based strictly on one-dimensional analysis, did not reveal the subtle but critical influence of the IGBT geometry on its transient turn-off characteristic. The constant $K_A<1$ in our model, although somewhat empirical, reflects this influence. Our analysis can further facilitate model parameter evaluation for IGBT circuit simulation. For example, it is possible to interpret a measured turn-off transient using our analysis and extract, for a given on-state current I_0, values for I_{MOS} (and hence β), τ_H, and J_{N0}. This utility should be of interest in the general area of CAD of HVICs.

CHAPTER 4
HIGH-VOLTAGE/POWER INTEGRATED CIRCUIT DEVICE MODELING--A FIRST APPROACH

4.1 Introduction

This chapter introduces a novel methodology for flexible SPICE2 implementation of physical models for HV/P IC devices developed in chapters 2 and 3. The model implementation is applied to the IGBT of Chapter 3 and is achieved without modification of the SPICE2 source code by utilizing UDCSs that access FORTRAN subroutines which define, implicitly, the current and charge as functions of the controlling node voltages. The implicit problem is numerically solved in a FORTRAN subroutine and its solution (a current or charge) is referenced by the SPICE2 main program. This highly flexible means (first approach) of model implementation differs from that presented in Chapter 5, where the implicit model equations are solved by the SPICE2 main program, thus trading model flexibility for computational efficiency. SPICE2 simulations of dc and transient characteristics of IGBT switching circuits are

shown to be representative of measurements taken from the literature. Both static and dynamic latch-up for the IGBT are simulated, thus demonstrating the flexibility of the modeling methodolgy for HV/P IC CAD.

Recent advances in silicon IC processing technologies have intensified development of "smart" high voltage/power (HV/P) circuits, in which low-power logic and high-voltage devices are integrated on the same chip. Computer-aided design (CAD) of such circuits is critically dependent on reliable device simulation, for example with SPICE2 [Na75]. HV/P devices have unique characteristics that are not amenable to lumped-element, equivalent-circuit representation, and hence the built-in device models in SPICE2 are generally inadequate. Such characteristics include effects of merging bipolar and MOS structures, latch-up, conductivity modulation, and moving-boundary (during transient) conditions. The inadequacy of the SPICE2 MOSFET models for HV/P IC simulations is clearly inferable from [Su80]. The SPICE2 BJT (Gummel-Poon [Ge78]) model is clearly deficient; for example, its basic (integral-charge-control [Ge78]) assumption is invalid for HV/P BJTs having significant back injection or relatively low currents gains.

Therefore to enable reliable CAD of HV/P ICs, new device models must be implemented in SPICE2, or in comparable circuit simulators. Because of the unique

device characteristics and model complexities, such implementation will require either modifying existing simulator codes to accommodate new specific models, or developing new methodologies for general model incorporation. This paper describes a simple, flexible and physical approach to the latter implementation. The methodoly is exemplified through an application to a representative device, the insulated gate transistor (IGBT) [Ba84b], an HV/P switch comprising merged bipolar and MOS structures. Although the (vertical) IGBT is not a common integrated device, we use it to demonstrate the modeling methodology, which is intended primarily for CAD of HV/P ICs, because (i) it is well documented, and (ii) its basic operation is not unlike that of other merged bipolar/MOS devices which are integrated, e.g., the lateral IGBT (LIGBT) [Ro86].

We stress that this chapter introduces and demonstrates a novel device modeling concept for HV/P circuit simulation, but does not include the simulation of any actual device nor a complete corroboration of model assumptions. The viability of the methodology is implied by the physical nature of the models and is shown through qualitative comparisons between model predictions and published measured characteristics.

The new SPICE modeling approach, presented in Section 4.2 and demonstrated in Section 4.3, utilizes expressions,

not necessarily in explicit form, for the quasi-static device terminal currents and charges (the models are charge-based) in terms of the terminal voltages. This system of equations, i.e. a physical device model, is part of a subroutine that is referenced by user-defined controlled sources (UDCSs) in SLICE [Ha84], one of the many enhanced versions of SPICE2 that have been written. The UDCSs generally available in enhanced versions of SPICE2, are simple FORTRAN subroutines [Ve86] that constitute the "equivalent-circuit" model, which simulates both steady-state and (quasi-static) transient device characteristics. With judicious programming and data storage, UDCSs can be used effectively for simulation of circuits in which the number of HV/P devices is not excessive.

4.2 Modeling Methodology

The utility of the novel methodoly is demonstrated by its application to the IGBT [Ba84b], as illustrated in Figure 4-1. The IGBT is representative of emerging HV/P devices that merge MOS and bipolar structures to exploit the advantages of both. The (n-channel) IGBT shown is effectively a vertical pnp BJT, the base of which is driven by a DMOST, with a parasitic npn BJT at the cathode that can cause latch-up and loss of gate control of the IGBT switch. In contrast to the conventional DMOST, the

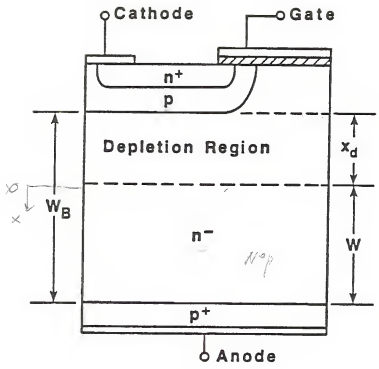

Figure 4-1. Basic IGBT structure.

conductivity of the n^- epitaxial region (base) of the IGBT is modulated by carrier injection from the p^+ anode (emitter), thereby lowering the on-resistance but also increasing the turn-off time because of the excess carrier storage. The device has been previously modeled [Yi85] by connecting numerical models for the DMOST and pnp BJT through a modulated base resitance. Such modeling aids optimal device design, but is impractical for circuit simulation and provides little insight into how device parameters affect the dynamic response of the IGBT in a circuit, or an HVIC.

We emphasize in this paper the SPICE simulation of the constituent wide-base (low-current-gain) pnp BJT and parasitic npn BJT. We thereby stress the inclusion in the model of unique characteristics like low BJT gain, base-region conductivity modulation, and latch-up, which are not properly accounted for in the built-in SPICE2 models. The DMOST is modeled using a standard level-2 SPICE2 MOSFET model [Ha84]. Because of the high level of conductivity modulation in the n^- base region, effects of the parasitic JFET [Yi85] at the drain of the DMOST can, to first order, be ignored when calculating the on-resistance. The methodolgy presented, however, is flexible enough to model the JFET effects if desired, but at the cost of increased model complexity.

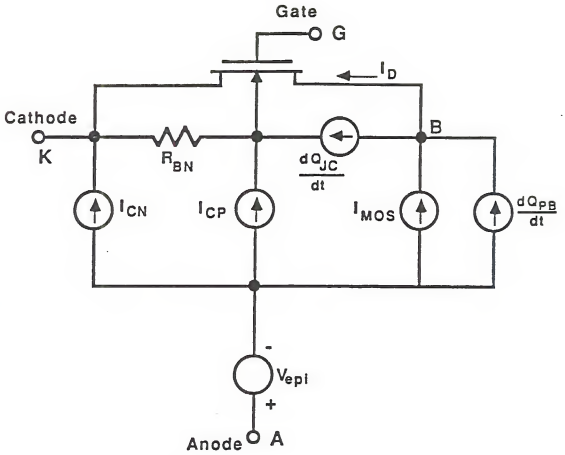

Figure 4-2. UDCS representation of the IGBT implemented in SLICE/SPICE2. This is not an equivalent circuit; the node B is labeled merely to signify the internal connection between the base region of the pnp BJT and the drain of the DMOST. The anode of the IGBT is referred to as the emitter of the pnp BJT, and the cathode as the collector.

The UDCS [Ve86] "circuit" model for the IGBT is shown in Figure 4-2. In fact, the model is not an equivalent circuit, but is a physical representation comprising six UDCSs, each of which is defined implicitly by the system of model equations in terms of the emitter-base and base-collector voltages (V_{AB} and V_{BK}) of the pnp BJT. The choice of node voltages used to define the UDCSs is not unique. Alternative choices, as demonstrated in Chapter 5, can be considered for a particular device to effect a trade-off among model flexibilty, complexity, and computational efficiency. The steady-state characteristics of the IGBT are simulated by the UDCSs I_{MOS} (the component of the pnp BJT base current supplied by the DMOST), I_{CP} (the pnp BJT collector current), and V_{epi} (the voltage drop across the n^- base region). The transient characteristics are simulated by the charge-based UDCSs [Ve86] dQ_{PB}/dt (the charging current defined by the carriers in the quasi-neutral base region of the pnp BJT) and dQ_{JC}/dt (the charging current defined by the depletion charge at the base-collector junction of the pnp BJT). Charging currents associated with free carriers in other regions of the device are typically negligible. For example, the charging current defined by the minority electrons in the quasi-neutral p^+ emitter (anode) region is negligible, even though the total pnp BJT base current ($I_{MOS} + I_{CN}$) must include a component due to recombination in the emitter, as shown in Chapter 3 [Fo86a]. The resistance R_{BN} simulates

the lateral voltage drop in the base region of the npn BJT, which is important only near latch-up as we discuss later.

The six UDCSs reference the same user-defined subroutine that defines the system of model equations. This set of equations is quasi-static; that is, Q_{PB} and Q_{JC}, as well as I_{MOS}, I_{CP}, I_{CN}, and V_{epi}, are described in the steady state in terms of V_{AB} and V_{BK}, and then the transient currents are characterized through the quasi-static approximation [Va76] which equates the time-dependences to the steady-state dependences in terms of $V_{AB}(t)$ and $V_{BK}(t)$. Virtually all device models used today for circuit simulation are quasi-static. Although we use the quasi-static approximation here, with some support for its validity, we recognize the need to consider the possible occurence of non-quasi-static (NQS) effects in each particular model development. Proper accounting for the NQS effects in SPICE models is a formidable task, but can be facilitated [Fo86b] by the new methodology presented in this chapter.

We now describe the physical model equations in detail. The sytem of equations is based on the solution to the one-dimensional ambipolar transport equation [Gh77] describing the carrier densities in the quasi-neutral n^- base region. Two-dimensional effects are considered later. Since the IGBT operates under high-injection (conductivity modulated) conditions in the n^- base region ($p \approx n >>$

N_{epi}), the base transport equation simplifies to

$$\frac{d^2p(x)}{d^2x} - \frac{p(x)}{L_A^2} = 0 \qquad (4\text{-}1)$$

where L_A [$=(D_A\tau_H)^{1/2}$] is the ambipolar diffusion length [Gh77]. The solution to (4-1), precluding a forward bias on the base-collector junction, is

$$p(x) = \frac{p(0)\sinh(\frac{W-x}{L_A})}{\sinh(\frac{W}{L_A})} \qquad (4\text{-}2)$$

where p(0) is the hole (or electron) density at the edge (x=0) of the emitter-base junction space-charge region and W is the effective base width. From Figure 4.1,

$$W = W_B - x_d \qquad (4\text{-}3)$$

where W_B is the metallurgical n^- base width and x_d, which is a function of V_{BK}, is the width of the depletion region at the one-sided base-collector junction of the pnp BJT. We define $x_d(V_{BK})$ based on the depletion approximation, and

neglect any mobile carrier charge that might exist in the space-charge region for very high current densities [Gh77].

To relate p(0) in (4-2) to V_{AB}, it is necessary to characterize V_{epi} since

$$V_{AB} = V_{epi} + V_{JEB} \tag{4-4}$$

where

$$V_{JEB} = V_T \ln\left[\frac{p(0)N_{epi}}{n_i^2}\right] \tag{4-5}$$

is the emitter-base junction voltage (not equal to the quasi-Fermi potential separation) [Wa83]. In (4-5), N_{epi} is the doping density in the n^- epitaxial base of the pnp BJT and $V_T = kT/q$ is the thermal voltage. Accounting for the conductivity modulation, we give V_{epi} by the integral of the electric field across the quasi-neutral base, where the field is related to p(x) through a combination of the hole and electron current expressions [Gh77]:

$$V_{epi} = \frac{J_A}{q(\mu_n+\mu_p)}\int_0^{W_M} \frac{dx}{p(x)} + \frac{(b-1)}{(b+1)}\frac{kT}{q}\ln\left(\frac{p(0)}{N_{epi}}\right) \tag{4-6}$$

where $W_M(\leq W)$ is defined by (4-2) as the point where p(x) equals N_{epi}; J_A is the anode (emitter) current density and $b=\mu_n/\mu_p$ is the electron/hole mobility ratio.

For negligible recombination in the emitter junction space-charge region, J_A is related to p(0) as follows [Be79]:

$$J_A = \frac{b+1}{b} \{J_{NO}[\frac{p(0)}{n_i}]^2 - qD_A \frac{dp}{dx}\Big|_{x=0}\} \qquad (4-7)$$

where D_A is the ambipolar diffusivity [Gh77] and J_{N0} is the saturation current density defined by the back injection of electrons into the quasi-neutral emitter region [Fo81].

Equations (4-4)-(4-7) relate p(0) to V_{AB} and V_{Bk}, the independent node-voltage differences in the model. Now (4-2) and (4-3) can be used with these relations, and the quasi-static approximation, to characterize the UDCSs in terms of these voltages. We note that although these characterizations are implicit, the model is implemented in SPICE2 directly via access of the UDCSs by the nodal analysis [Ve86].

The UDCS V_{epi} is given by (4-6). The quasi-static depletion charge density at the base-collector junction is

$$Q_{JC} = qAN_{epi}x_d \qquad (4-8)$$

where A_C is the (effective) base-collector junction area. The quasi-static carrier charge in the quasi-neutral base region is the integral of (4-1) from x=0 to x=W:

$$Q_B = qA \int_0^W p(x)dx \qquad (4\text{-}9)$$

where A_E is the emitter, or anode, area. The charging-current UDCSs in the model are derived from (4-8) and (4-9):

$$\frac{dQ_i}{dt} = \sum_j \frac{\partial Q_i}{\partial V_j} \frac{dV_j}{dt} \qquad (4\text{-}10)$$

where i=JC, PB and j=AB, BK. Therefore the "transcapacitance" $\partial Q_i/\partial V_j$ must also be described in the UDCS, either analytically or numerically. We note from (4-9) and (4-10) that the transcapacitances associated with Q_{PB} cannot be described in closed form, and hence finite-difference approximations are used in the UDCS dQ_{PB}/dt to characterize them numerically.

The composite base current I_B of the pnp BJT, in the steady-state, is the sum of recombination current from the n^- base region and that from the p^+ emitter region. It is expressed as

$$I_B = \frac{Q_{PB}}{\tau_H} + A_E J_{N0} [\frac{p(0)}{n_i}]^2 \qquad (4\text{-}11)$$

where τ_H is the high-injection carrier lifetime [Gh77] in the base. The second term in (4-11) obtains for quasi-equilibrium because low injection prevails in the emitter. The electrons that support the recombination current I_B are supplied by the DMOST (I_{MOS}) under normal operation, but in part also by the npn BJT (I_{CN}) near latch-up:

$$I_{MOS} = I_B - I_{CN} \; . \qquad (4\text{-}12)$$

Analytical decomposition of I_B, as well as characterization of the n^- base transport current I_{CP}, must be done implicitly and hence demonstrates poignantly the essence (flexibility) of the modeling methodolgy, in contrast to the less-flexible equivalent-circuit modeling built into SPICE2.

The lateral flow of the collected holes I_{CP} in the base of the npn BJT forward-biases the emitter-base junction and causes electrons to be injected into the base of the pnp BJT (see Figure 4-1). This p-base transport current can be approximated by [Ha85]

$$I_{CN} = I_{SN} \exp(\frac{I_{CP}R_{BN}}{V_T}) \qquad (4\text{-}13)$$

where I_{SN} is the collector saturation current of the npn BJT and R_{BN} is an average, or lumped, base resistance [La85], both of which vary inversely with the p-base Gummel number [Ge78]. However note that because of the exponential dependence of I_{CN} on I_{CP}, only for conditions near latch-up is the contribution of I_{CN} to the anode current $I_A=A_EJ_A$ significant. When $I_{CN}\simeq 0$, $I_{MOS}\simeq I_B$ and the DMOST supplies all the electrons necessary for recombination in the pnp BJT. However when the IGBT is latched, the electrons necessary for recombination are supplied by the npn BJT (I_{CN}), and $I_{MOS}\simeq 0$.

The implicit description of the current UDCSs is completed by equating the pnp BJT collector current (I_{CP}) to the difference between the emitter current (I_A) and the base current (I_B):

$$I_{CP} \simeq \frac{A_C}{A_E}(I_A - I_B) \ . \qquad (4\text{-}14)$$

In (4-14), and in (4-8), (4-9), and (4-11), we have crudely accounted for the two-dimensionality of the pnp BJT by including the (constant) collector-emitter area ratio, which is less than unity. Although this accounting is semi-empirical , it does reflect the reduced base transport factor in a typical IGBT due to hole injection into a portion of the base that is laterally removed from the collector, as shown in Chapter 3 [Fo86a]. Model predictions made without the area ratio do not compare favorably with experimental results, whereas those made with it do. We note that for lateral devices,discussed in Chapter 5, however, a more physical accounting for the multidimensional effects is essential.

Because of the implicit nature of the model equations (4-2)-(4-14), it is not possible to express p(0), and hence the terminal currents, as explicit functions of V_{AB} and V_{BK}. Thus, for a given V_{AB} and V_{BK} supplied by the SPICE2 nodal analysis, (4-4) is solved iteratively (Newton's method) for p(0) in a FORTRAN (UDCS) subroutine, and the model equations are then used to determine I_{MOS}, I_{CP}, I_{CN}, V_{epi}, Q_{PB}, and Q_{JC}. The model is clearly quasi-static; at each point in time, the steady-state model equations are solved in a UDCS subroutine and the solution (a terminal

current or charge density) is then referenced by the main SPICE2 nodal analysis program [Ve86]. We note that in addition to the transcapacitances in (4-10), the transconductances $\partial I_i/\partial V_j$ for each current UDCS must be evaluated in the nodal analysis. These evaluations are done numerically using first-order finite-difference approximations.

The merged structure of the IGBT makes model parameter evaluation difficult because of two-dimensional current flow and inaccessibility of internal model nodes for measurement. Model parameters for the DMOST and BJT components of the IGBT can be estimated from a knowledge of processing variables, doping density profiles, and geometry. The threshold voltage for the DMOST can be estimated from measurements of $I_A(V_{GK})$, although the channel conductance cannot be inferred experimentally without a special test structure. The two most important parameters for the pnp BJT are τ_H and J_{N0}. As will be shown in Section 4.3, these two parameters greatly influence the steady-state on-resitance and turn-off time of the IGBT. From a knowledge of the pnp BJT emitter doping density, J_{N0} can be estimated analytically [Fo81]; and τ_H can be obtained from a fitting of a measured turn-off transient once J_{N0} is known, as described in Chapter 3. For the npn BJT, I_{SN} and R_{BN} can be estimated from a knowledge of the p-base doping density, or Gummel

number [Ge78]. Parameter exractions from latch-up measurements could be done, but would not be straight forward because of the difficulty in isolating important current components, e.g., I_{CP}.

4.3 SPICE Simulations and Discussion

In this section we demonstrate the utility of the modeling methodology used to develop the SPICE IGBT model in Section 4.2. Results of representative IGBT circuit simulations on SPICE are presented and discussed. Figure 4-3 shows simulated dc IGBT current-voltage characteristics for various values of gate-to-cathode voltage, V_{GK}. Typical parameter values were used for these simulations, and the results shown are representative of typical vertical IGBTs. For V_{GK} sufficiently high, the DMOST operates in the linear region, and the I_A-V_{AK} relationship, where V_{AK} is the anode-cathode voltage, is linear. This linearity indicates that the on-resistance of the IGBT in this case is not affected by the nonlinear V_{epi}, but is controlled by the DMOST channel conductance and by contact resistance. For lower V_{GK}, I_A tends to saturate with increasing V_{AK}. This saturation occurs because the DMOST is driven to the saturation region, and therefore I_{MOS} ($\approx I_B$), and hence I_{CP} are limited. For V_A less than about 0.6 V, the IGBT does not conduct any appreciable current because the unmodulated n^- epi resistance is so large; N_{epi}

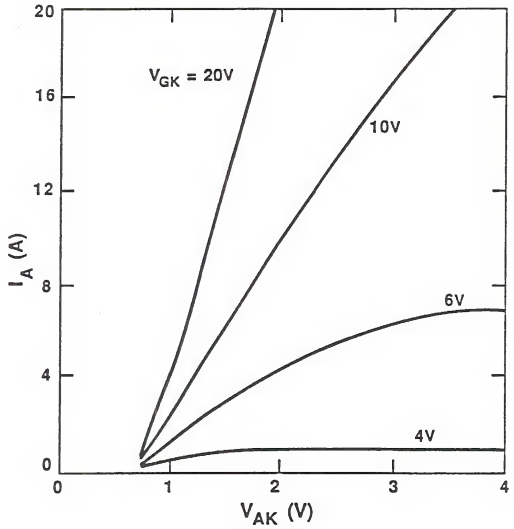

Figure 4-3. Simulated IGBT anode current versus anode-cathode voltage for various gate-cathode voltages. The DMOST threshold voltage is 3 V.

is low to provide high voltage blocking. A forward bias of approximately 0.6 V is required to produce high injection and conductivity modulation, which lowers the resistance of the epi region. Our model equations are valid only in this region of operation; for low-injection conditions, I_A is in the milliamp-range and is well below any current of practical concern. No attempt has been made to model the reverse-blocking mode of operation, where $V_{AK}<0$. The methodology is flexible and this region of operation could be modeled by including UDCSs, or modifying existing ones to account for the leakage (generation) current associated with the reverse-biased emitter junctions of the npn and pnp BJTs. In this extension, the effects of an n^+ buffer layer at the anode, modeled for the GDS in Chapter 2, would have to be included.

To exemplify transient IGBT simulations, we use the representative gate-drive circuit [Ba84c] shown in Figure 4-4. The diode isolates the pulse generator during turn-off transients. The impedance Z_L repesents a load on the IGBT, which typically is resistive, inductive, or a combination of both. The resistor R_{GK} provides a path to discharge the gate-to-cathode capacitance; it influences the turn-off characteristic by limiting the rate of change of V_{GK}, and hence limits the rate of change of the anode current, I_A. If R_{GK} is sufficiently small (~10Ω), then depending on the steady-state value of I_A, the IGBT may

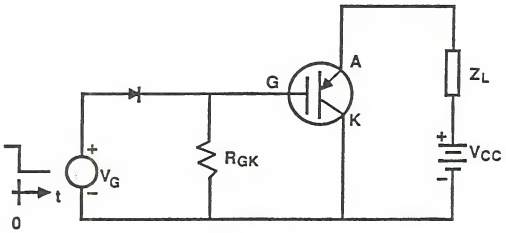

Figure 4-4. Gate-drive circuitry for IGBT transient simulations. The pulse voltage, V_g, was defined to fall from 10.7 to zero in 50 ns. The voltage V_{cc} was set at 350 V.

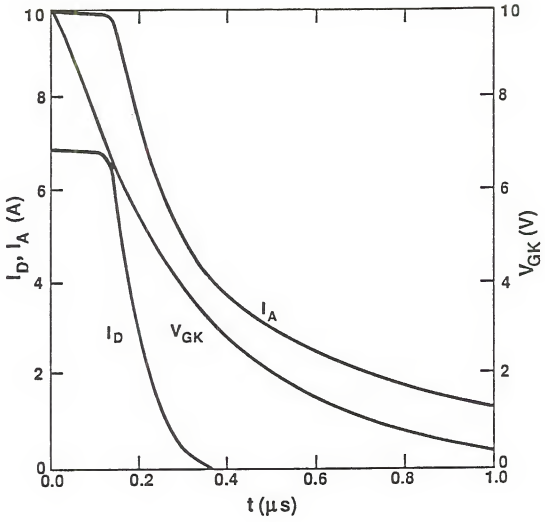

Figure 4-5. IGBT anode current, DMOST drain current, and gate-cathode voltage versus time from simulation of turn-off transient defined in Figure 4-4 with resistive load Z_L = 35 Ω and R_{GK} = 200 Ω (τ_H = 0.8 μs, J_{NO} = 10^{-12} A/cm^2).

latch during turn-off. Mechanisms that produce latch-up in the IGBT will be simulated and discussed later.

In Figure 4-5 we show a simulated turn-off transient for a typical IGBT in Figure 4-4 with a resistive load. The turn-off delay reflected by $I_A(t)$ results because of the finite time needed to discharge the gate-to-cathode capacitance of the DMOST, and is a function of R_{GK}. This discharging time is evident in the $V_{GK}(t)$ decay shown, which is much slower than the fall of the $V_G(t)$ pulse. Note that $V_{GK}(t)$ influences $I_A(t)$ by controlling the conductance of the DMOST. As shown in Figure 4-5, the DMOST transient drain current, $I_D(t)$, which, from Figure 4-2, equals $I_{MOS} + dQ_{PB}/dt - dQ_{JC}/dt$, does not begin to fall until $V_{GK}(t)$ has decreased to a value that causes the DMOST to saturate (see Figure 4-3). Further reduction of $V_{GK}(t)$ decreases the DMOST (saturation) current $I_D(t)$, and hence $I_A(t)$ as well. Eventually $V_{GK}(t)$ becomes less than the DMOST threshold voltage, and $I_D(t)$ drops to zero. $I_A(t)$, which includes $I_D(t)$, follows the decrease in $I_D(t)$ until it becomes a negligible component, after which $I_A(t)$ decays in accordance with the recombination in the pnp BJT [Fo86a]. If V_{GK} is reduced very rapidly, for example by decreasing R_{GK}, then I_D falls to zero very quickly, resulting in the more idealized two-phase turn-off transient [Fo86a,Ba85,Ku85] shown by simulation in Figure 4-4. In contrast to previous analytical results

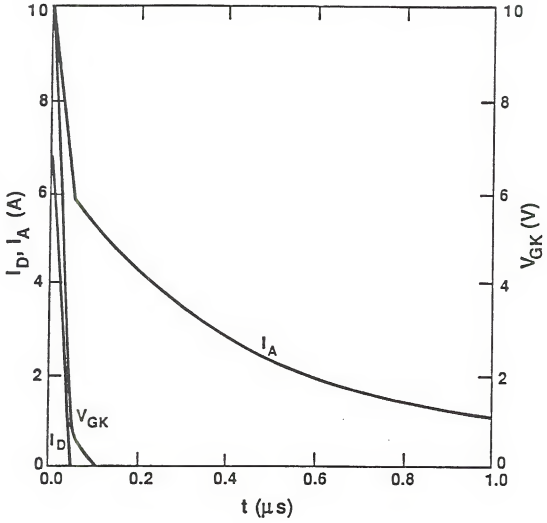

Figure 4-6. IGBT anode current, DMOST drain current, and gate-cathode voltage versus time from simulation of turn-off transient defined in Figure 4-4 with resistive load Z_L = 35 Ω and R_{GK} = 5 Ω (τ_H = 0.8 μs, J_{NO} = 10^{-12} A/cm^2).

[Ba85,Ku85], our SLICE/SPICE2 simulations show that the abrupt drop in $I_A(t)$ is not equal to the steady-state DMOST current $I_D=I_{MOS}$ (even when I_{CN} is zero), and that the slow decay of the second phase is not a simple exponential function of the high-injection lifetime τ_H. These differences result, respectively, from the unique effects of the expanding depletion region at the base-collector junction and the back injection of electrons into the emitter characterized by J_{N0}, poignantly demonstrated in Chapter 3.

In Figure 4-7 we show simulated IGBT resistive turn-off transients for various values of τ_H and J_{N0}. To stress the influence of these parameters, we used a small value for R_{GK} that ensured the insignificance of transients associated with the gate-to-cathode capacitance. The magnitude of the fast initial drop in anode current and subsequent slower decay are both dependent on τ_H and J_{N0}. These simulations and others have shown that changes in J_{N0} should be considered as a means of optimizing the trade-off between turn-off time and on-resistance. We stress that these results could not be obtained using standard SPICE2 BJT models because of the limitations inherent in the Gummel-Poon model [Ge78] and its implementation in SPICE2.

We stress that the results in Figure 4-7 are ideal in that, in addition to negligible gate delay, there is also no inductance in the load. For contrast, we show in

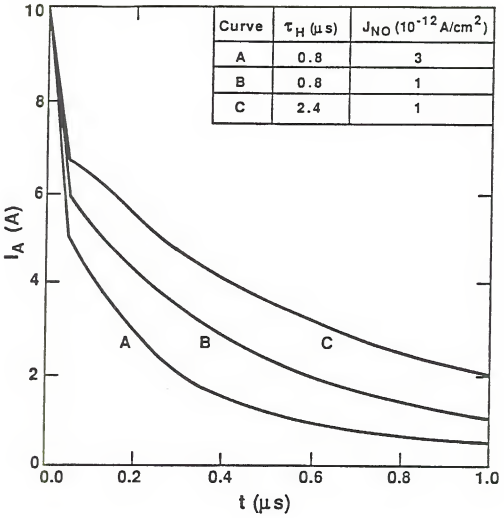

Figure 4-7. IGBT anode current versus time from simulation of resistive turn-off transient for various values of τ_H and J_{NO} (R_{GK} = 5 Ω).

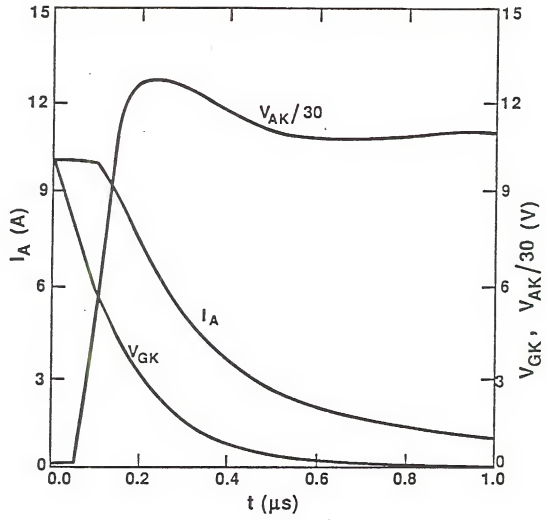

Figure 4-8. IGBT anode current, (normalized) anode-cathode voltage, and gate-cathode voltage versus time from simulation of turn-off transient with inductive load. In Figure 4-4, Z_L is a series combination of 8 μH and 35 Ω; R_{GK} = 100 Ω.

Figure 4-8 a simulated turn-off transient for an IGBT in Figure 4-4 with an inductive load, including a gate delay. A distinctive characteristic of this turn-off transient is the sharp rise of the anode-to-cathode voltage $V_{AK}(t)$, which even shows overshoot and ringing as do corresponding measurements [Ba84c]. This unique $V_{AK}(t)$ transient results from a damped resonance defined by the load inductance in combination with the junction capacitance repesented by the charging current dQ_{JC}/dt in our model.

To further demonstrate the utility of the modeling methodology, we simulate the static latch-up of a representative IGBT, but with a larger npn BJT base resistance R_{BN}. As mentioned previously, the IGBT may latch, causing loss of gate control, if driven too hard. For the static case, depicted in Figure 4-9 by the simulated $I_A(V_{AK})$, latch-up is approached by increasing I_A. As characterized in Section 4.2, I_{CP} also increases, and subsequently, because of the increased forward bias $I_{CP}R_{BN}$ on the emitter-base junction of the npn BJT, so does I_{CN}. At the onset of latch-up, I_{CN} increases abruptly, thereby reducing I_{MOS} in accordance with the recombination in the pnp BJT. The reduction of I_{MOS} decreases the voltage dropped across the DMOST and results in the negative-resistance region shown in Figure 4-9. The process is regenerative, and as the applied current is increased further, ultimately I_{CN} supplies all the

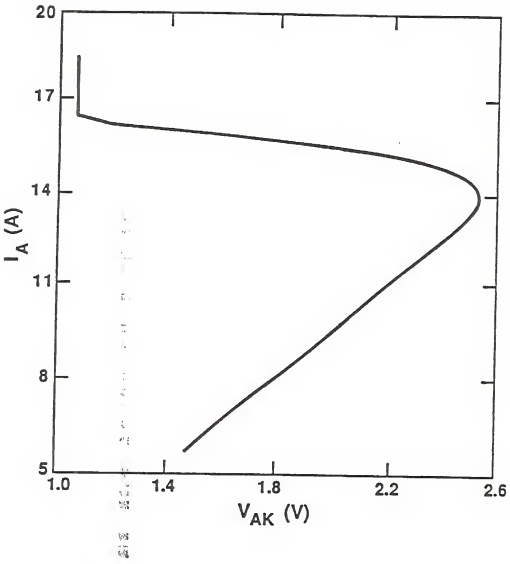

Figure 4-9. Simulation of static latch-up in the IGBT: driving anode current versus the resulting anode-cathode voltage with gate-cathode voltage equal to 10 V (I_{SN} = 2 x 10^{-12} A and R_{BN} = 0.175).

electrons supporting the recombination current in the pnp BJT, and I_{MOS} is reduced to zero. In this condition, the device is latched, and removal of the gate voltage will have no effect on the I_A. The transition from a stable operating point to the latched condition requires only a small increase in applied current because of the exponential dependence of I_{CN} on I_{CP}.

The IGBT can also latch during turn-off transients if the lateral hole current in the base of the npn BJT, which, at the start of the transient, consists of I_{CP} plus the displacement current dQ_{JC}/dt, is sufficiently high to effectively forward-bias the npn BJT emitter-base junction. The magnitude of dQ_{JC}/dt depends on the rate of change of the gate-to-cathode voltage as defined by the IGBT model and the external circuitry. In the ideal case, if V_{GK} is removed instantaneously, then the initial magnitude of dQ_{JC}/dt is equal to the steady-state current I_{MOS} supplied by the DMOST, as discussed Chapter 3 [Fo86a]. If V_{GK} is removed slowly, then the initial magnitude of dQ_{JC}/dt will be negligible, and the IGBT will not latch. In Figure 4-10 we show a simulation of dynamic latch-up in the IGBT, which occurs because $V_{GK}(t)$ drops abruptly (due to a small R_{GK} as discussed previously). The turn-on of the BJT, which triggers the latch-up, is indicated by the rapid increase in its collector current $I_{CN}(t)$ shown in Figure 4-10. Beyond this point in time, $I_A(t)$ remains finite even though $V_{GK}(t)$ has dropped to zero.

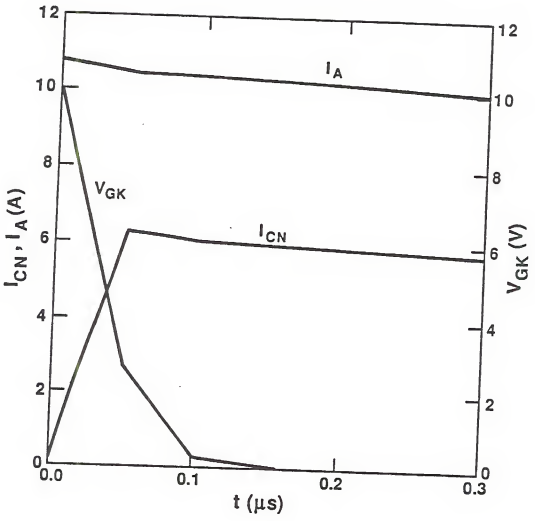

Figure 4-10. Simulation of dynamic latch-up in the IGBT: anode current, npn BJT collector current, and driving gate-cathode voltage versus time with R_{GK} = 15 Ω (I_{SN} = 2 x 10^{-12} A and R_{BN} = 0.175 Ω).

4.4 Summary

A methodology for SPICE implementation of high-voltage/power integrated circuit device models has been presented and demonstrated. The methodology is flexible and enables an accounting for the unique characteristics associated with HV/P IC devices, such as merging bipolar and MOS structures, latch-up, conductivity modulation, and moving boundary conditions. A representative HV/P device, the IGBT, was modeled using a system of implicit equations relating the quasi-static device terminal currents and charges to the terminal voltages. The physical IGBT model was implemented in SLICE/SPICE2 by using UDCSs, simple FORTRAN subroutines referenced in the SPICE2 nodal analysis. Simulations of IGBT circuits, reflecting dc and transient characteristics of the HV switch were described. These simulations, which included static and dynamic latch-up, are not possible with built-in SPICE2 lumped-element models, and thus poignantly demonstrate the need for and utility of the new flexible and physical modeling methdology. CPU times required to do the simulations with the UDCS model are substantiallly longer than times for (invalid) simulations with built-in models in SPICE2. However they are not prohibitive for small-scale circuits; typically the new models necessitated CPU times, for both dc and transient simulatons, about an

order-of-magnitude longer than those for the built-in models. For larger-scale HVICs, new HV/P device models, once they are developed and standardized based on the methodolgy presented in this paper, could be written into the SPICE2 code to reduce CPU times to acceptable values.

CHAPTER 5
HIGH-VOLTAGE/POWER INTGRATED CIRCUIT DEVICE MODELING

5.1 Introduction

This chapter combines and extends much of the work and insight gained in previous chapters. In this chapter, new physical models, and a general modeling methodology, for lateral HV/P devices, in particular LIGBT structures, are developed, and the models are implemented in SPICE via UDCSs. The models are charge-based, and via regional partitioning, account for the unique features of lateral HV/P devices (multidimensional carrier flow, conductivity modulation, latch-up, transcapacitance) unaccounted for in conventional equivalent-circuit models. Device measurements of specially designed test structures, supplemented with two-dimensional numerical device simulations, support the modeling methodolgy and the model parameter extraction.

The implementation of the models in the circuit simulator is flexible, and differs from the implementation in Chapter 4 in that the model is implicitly formulated

such that the circuit simulator derives the solution to the implicit nonlinear system of equations. In Chapter 4, the implementation required the implicit system of model equations to be solved by a FORTRAN algorithm accessed by the SPICE nodal analysis, and consequently the implemented SPICE model was computationly inefficient. The new implementation presented in this chapter, although not as flexible as that of Chapter 4, is nearly twenty times faster.

We describe in this chapter the development of new models for HV/P devices, in particular for lateral IGBT [Da84,Pa86,Mc87,Si85] structures which are representative of the HV/P devices in power ICs. The models are physical, yet are implemented in SPICE, as we describe, through flexible techniques which do not require sacrificing physics through excessive empiricism. Thus the models can be used to aid optimal device (process) design as well as for CAD of HV/P ICs.

In the application of the modeling methodolgy to the LIGBT, the device is regionally partitioned into three one-dimensional bipolar transistors (BJTs) coupled to the DMOS transistor, yielding a quasi-two-dimensional model for the LIGBT. The consistuent device structures are reresented by physical charge-based models in which currents and charges are related to junction voltages implicitly by sets of equations derived by solving the

pertinent ambipolar transport problems. Charging currents in the transient model are represented by time-derivatives of the quasi-static charges, which implicitly (without capacitors) account for charge conservation and nonreciprocal transcapacitance.

The models are implemented in SPICE via user-defined controlled sources (UDCSs), which are FORTRAN subroutines accessed by the SPICE nodal analysis. The UDCSs define the systems of model equations, which are analytic but must be solved simultaineously and hence numerically. The solution of the equations is derived by the nodal analysis.

The LIGBT model and the methodology are supported by measurements of specially designed test structures, which also support the model parameter extraction. This verification is facilitated by two-dimensional numerical device simulations with PISCES [Pi84] that provide needed physical insight regarding, for example, current-crowding effects, and imply how the partitioning of the LIGBT should be done to effectively account for coupling among the constituent devices. The test devices are lateral structures designed to allow experimental access to different regions of the LIGBT, for different modes of operation, i.e., as a DMOS transistor, as an IGBT, or as a "hybrid LIGT/DMOST" (HIGBT) [Si85,Fo87] with the anode terminal shorted to the DMOST drain. This latter mode of operation depends on an internal voltage drop to

forward-bias the anode junction and activate the IGBT. The test structures were fabricated using a dielectric-isolation process [Go78] which eliminates parasitic substrate effects. The utility of the flexible and physical modeling is emphasized by SPICE simulations of the LIGBT which reflects the three possible active modes of operation. Furthermore, the onset of both static and dynamic latch-up can be be simulated straightforwardly with the physical SPICE model.

5.2 Modeling Methodolgy

We demonstrate the modeling methology through an application to the LIGBT structure illustrated in Figure 5-1. The fabrication of this specially designed device is described in Section 5.3. To develop a quasi-two-dimensional model, we partition the structure into one-dimensional constituent componenets as indicated in Figure 5-1. The basis for this partitioning rests upon physicl insight gained from device measurements in the various modes of operation (PIN, DMOST, LIGBT, HIGBT) and from device simulations using PISCES. Subdividing a multidimensional structure into coupled one-dimensional devices is not uncommon [Li67], but in this case of HV/P devices the empiricism implied must be minimized through proper accounting for the underlying physics. The unique effects of significant back injection, base-region conductivity modulation, and the associated low current

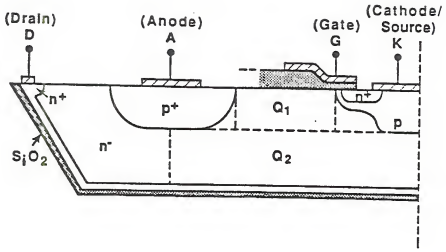

Figure 5-1. Special LIGBT test structure (symmetric about the axis shown). The spacing between the 10 μm deep p^+ anode and the cathode is 78 μm. The thickness of the n^- (5×10^{14} cm^{-3}) layer is 35 μm and the depth is 300 μm.

gain in the BJT modules, which invalidates the commonly used SPICE Gummel-Poon model [Ge78], necessitate new (more physical) models.

We first focus our attention on the one-dimensional low-gain pnp BJT constituent module (see Figure 5-1), and overview the development given in Chapter 4. The low doping density in the wide n^- base region implies that, under normal forward-mode operation, high injection will prevail throughout the base. Consequently, the base transport problem is described by the ambipolar transport equation with p=n, the solution of which gives

$$n(x) \simeq p(x) = \frac{p(0)\sinh(\frac{W-x}{L_A})}{\sinh(\frac{W}{L_A})} \qquad (5\text{-}1)$$

where p(0) is the hole density at the edge of the emitter-base (p^+n^-) junction space-charge region, L_A is the ambipolar diffusion length, and W is the voltage-dependent width of the quasi-neutral base region. We describe W through the depletion approximation at the reverse-biased collector-base (pn^-) junction:

$$W = W_B - x_d \qquad (5\text{-}2)$$

where W_B is the metallurgical base width and $x_d=[\varepsilon_S(\phi+V_{BC})/qN_{epi}]^{1/2}$ is the (one-sided) collector-base (step) junction depletion-region width. In writing (5-1), we have assumed that the simplified ambipolar transport equation ($p\approx n$) is valid over the entire quasi-neutral base region and thus, as done in [Fo77], we have implicitly neglected the effects of the relatively narrow low-injection region near the collector. In addition, consistent with PISCES simulations for typical operating conditions, the effects of mobile carriers in the collector-base junction space-charge region, viz., quasi-saturation [Je87], have been neglected. Indeed in the wide-base transistor, the base widening associated with quasi-saturation is negligible.

In contrast to the Gummel-Poon model, our (low-β) module properly accounts for, via (5-1), possibly substantial recombination in the base region. Furthermore, the module must account for possibly substantial recombination in the p^+ emitter region as well as a current-induced electric field in the conductivity-modulated base region which arises to support the quasi-neurality. The integral of this electric field across the base region defines a voltage drop, V_{epi}, which causes the emitter-base junction voltage, V_{JEB}, to be less than the applied terminal voltage, V_{EB}:

$$V_{EB} = V_{JEB} + \frac{J_E}{q(\mu_n+\mu_p)} \int_0^{W_M} \frac{dx}{p(x)} + \frac{(b-1)}{(b+1)} \frac{kT}{q} \ln\left(\frac{p(0)}{N_{epi}}\right) \qquad (5\text{-}3)$$

where $W_M<W$ is defined by (5-1) as the point where $p(x)$ equals N_{epi}, the base-region doping density J_E is the emitter (anode) current density, and $b \triangleq \mu_n/\mu_p$ is the electron/hole mobility ratio. (We generically refer to the n^- base region as also the epi region, even though it may not have been produced by epitaxial growth as in the case for our devices modeled in Section 5.3.)

Using the quasi-equilibrium assumption, we express $p(0)$, and hence V_{epi}, in terms of V_{JEB}:

$$p(0) = \frac{n_i^2}{N_{epi}} \exp\left(\frac{qV_{JEB}}{kT}\right) \quad . \qquad (5\text{-}4)$$

(If in a simulation $p(0)$ is calculated to be less than or equal to N_{epi}, the model is defaulted to the off-state since the high-injection analysis is inapplicable.) For negligible recombination in the emitter-base junction space-charge region, J_E can be related to $p(0)$ following conventional PIN-diode theory [Be79]:

$$J_E = \frac{b+1}{b} \left\{ J_{NO}\left[\frac{p(0)}{n_i}\right]^2 - qD_A \left.\frac{dp}{dx}\right|_{x=0} \right\} \qquad (5\text{-}5)$$

where D_A is the ambipolar diffusivity, and J_{N0} is the saturation current density that defines the back injection of electrons into the quasi-neutral eitter region. The base current density, J_B, is the sum of the back injection current plus the integrated recombination current in the base region:

$$J_B = J_{N0}[\frac{p(0)}{n_i}]^2 + q \int_0^W \frac{p(x)}{\tau_H} dx \qquad (5\text{-}6)$$

where τ_H is the high-injection carrier lifetime [Note that $L_A=(D_A\tau_H)^{1/2}$]. The collector current density, J_C, is expressed as J_E-J_B. The cross-sectional area A relates the terminal currents I_E and I_C (and I_B) to the respective current densities.

The transient modeling of the transistor is done using a charge-based method employing the quasi-static approximation. This approximation, which is used extensively for IC modeling [Ge78], is generally adequate except for circuits much faster than typical power ICs [Fo86b].

The predominant charges in the wide-base BJT module (in the forward-active mode) are the quasi-neutral

base-region charge Q_B and the collector-base junction depletion-region charge Q_{JC}. For quasi-static conditions, Q_B is given by the integral of (5-1) from x=0 to x=W:

$$Q_B = qA \int_0^W p(x)dx \ ; \qquad (5\text{-}7)$$

and

$$Q_{JC} = qAN_{epi}x_d \ . \qquad (5\text{-}8)$$

The charging currents are derived from (5-7) and (5-8):

$$\frac{dQ_i}{dt} = \sum_j \frac{\partial Q_i}{\partial V_j} \frac{dV_j}{dt} \qquad (5\text{-}9)$$

where i=B,JC and j=JEB,BC. The transcapacitances, $\frac{\partial Q_i}{\partial V_j}$, in (5-9) can be nonreciprocal, and hence the charge-based model is more representative of the actual charge dynamics than a conventional capacitance-based model.

Our low-β BJT (with wide, lightly doped base) module differs significantly from the conventional Gummel-Poon

model in several ways that make it physically representative of high-voltage devices. The charge-based formalism (5-9) properly accounts for transcapacitances, which cannot be represented faithfully by reciprocal capacitors [Fo86b]. The base-region voltage drop V_{epi} in (5-3) is modeled directly and generally (even for $\beta<1$, viz., very high J_B). The relationship (5-5) from PIN-diode theory ensures the proper simulation of the emitter efficiency for high-injection conditions in the base region. For example in the limit of very high injection, the model with (5-5) correctly predicts $\beta \rightarrow 1/b \equiv \mu_p/\mu_n$ (base-region mobilities). Thus, high-voltage p^+n^-p and n^+p^-n BJTs have different limiting current gains (Appendix A).

The network representation of the charge-based low-β pnp BJT module is shown in Figure 5-2. The module is implemented in SPICE via user-defined controlled sources (UDCSs) [Ve86] in a novel manner which allows the circuit simulator to solve the nonlinear equations implied by (5-1)-(5-8). UDCSs are FORTRAN subroutines in SLICE [Ha84], an enhanced version of SPICE2. Each element of the module is a UDCS that describes the current (and associated transconductance or transcapacitance calculated numerically using finite-difference approximations) via the system of equations described above (Appendix B). The SPICE nodal analysis accesses the subroutines iteratively in the

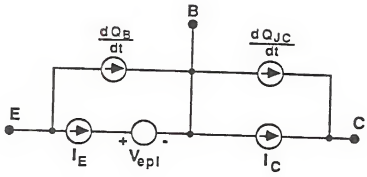

Figure 5-2. Charge-based network representation for a wide-base, low-β pnp BJT.

simulation process. This implementation of an implicitly formulated model allows for flexibilty in the modeling methodolgy, and enables truly physical device models to be incorporated into the device simulator.

We now exemplify the modeling methodogy by applying it to the LIGBT test structure, and partitioning the structure into one-dimensional modules for each mode of operation.

5.3 Application/Demonstration

Test structure of LIGBTs were fabricated using the dielectric-isolation (DI) BCMOS technology [Go87] developed at ATT Bell Laboratories. The LIGBT is dielectrical isolated from the substrate and from other components to minimize parasitic effects, thus allowing access to the drain of the DMOST separately from the anode of the LIGBT and making it easier to measure electrical parameters of the structure. This facilities the demonstration of our modeling methology, including the parameter extraction and comparisons between model predictions and device measurements.

The LIGBT structure shown in Figure 5-1 can operate in several modes (PIN, DMOST, LIGBT, HIGBT) depending on the terminal configuration. We must therefore develop a systematic and consistent approach to modeling the various modes of operation. The physical nature of our constituent modules facilitates parameter extraction by minimizing the

empirical optimization needed. In addition, the modular approach allows for a straightforward network representation of the LIGBT structure as will be shown in this section. We note that in all cases, the simulation of the actual symmetrical device involves area doubling of the model derived from the half-structure shown in Figure 5-1.

With the cathode floating, the drain tied to ground and the anode biased to a positive voltage, the LIGBT structure operates as a forward-biased PIN-diode. The PIN-diode current-voltage characteristic can be used to obtain information regarding recombination properties of the n^- epi region (τ_H) and of the p^+ anode region (J_{N0}). An optimization program was written to extract from measured I-V characteristics the three adjustable parameters (τ_H, J_{N0}, and J_{P0}, the cathode counterpart of J_{N0}) of a one-dimensional PIN-diode model [Mc85]. The optimization yielded τ_H=2.6μs and J_{N0}=6X10^{-13} A/cm^2 at room temperature. These parameter values were found to be commensurate with measured turn-off transients of the LIGBT, discussed below.

In the DMOST mode, the anode is left floating and the drain is set at a positive voltage relative to the source (cathode). The DMOST is empirically modeled as a simple MOSFET (SPICE/level 2 [Ha84]) with a resistor, R_{epi}, tied to the drain which accounts for the large n^- epi resistance. Although this model is inadequate in general,

it suffices here for assessing the validity of the modeling methodology applied predominantly to the bipolar aspects of the LIGBT. Fitting this model to the measured linear-region transconductance, we extract values for R_{epi} (325 Ω), the threshold voltage (2.6 V), and the transconductance factor ($1.9X10^{-3}$ A/V).

In the LIGBT mode, the drain is left floating and a positive voltage is applied to the anode. With the gate biased above the threshold voltage, the n-channel supplies base current for the lateral p^+n^-p BJT. Our quasi-two-dimensional modeling of this transistor is done by partitioning it into two one-dimensional transistors, Q_1 and Q_2, each represented by BJT modules described in Section 5.2. The partitioning is defined based upon results we obtained from PISCES simulations, which show that the ratio of lateral-to-vertical injection from the p^+ anode (emitter) is nearly excitation-independent. Figure 5-3 shows a typical PISCES result for the hole current distribution in our test structure for the LIGBT mode of operation. The one-dimensional current flow in the center section of the structure is clearly seen and demonstrates that the quasi-two-dimensional modeling via partitioning is a viable approach. The active area and base width for Q_1 are defined by the anode diffusion depth and the geometry, as illustrated in Figure 5-1. The base width and area for Q_2 are defined to make the simulated current agree with

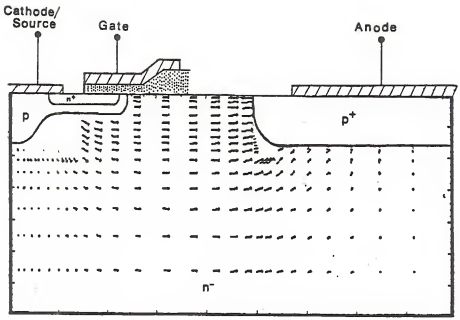

Figure 5-3. PISCES simulation for the LIGBT structure shown in Figure 5-1. The arrows indicate the negative hole current vectors. The current vectors around the junctions (high grid density) have been removed for illustrative clarity.

experimental results. To first order, they may be estimated from PISCES results. This particular partition is indeed representative of the device as implied by (a) PISCES simulations, (b) experimental decomposition of current voltage characteristics, and (c) relative excitations of Q_1 and Q_2 in the hybrid HIGBT mode of operation discussed later.

The SPICE model for the LIGBT mode is shown in Figure 5-4. It consists of a simple MOSFET and 11 UDCSs. The UDCSs labeled with the subscript one represent Q_1 and those with the subscript two represent Q_2. The current source I_{CNPN} models the third constituent BJT at the cathode as it, when activated by the voltage drop in the p-base reflected by R_{pB}, effects the onset of latchup, which is discussed later.

In the hybrid HIGBT mode of operation, the anode and drain are tied together and raised to a positive voltage relative to the source. The gate voltage, as in the the LIGBT mode, is above the threshold voltage. For low drain voltages, the device behaves as a DMOST, in series with a large resistance, R_{epi}. The anode does not inject because it is at the same potential as the drain. As the drain current through R_{epi} is increased, an internal voltage drop develops (vertically in this particular device) across a portion of the epi region. When this voltage drop becomes approximately 0.6V (viz., a diode drop) a portion of the

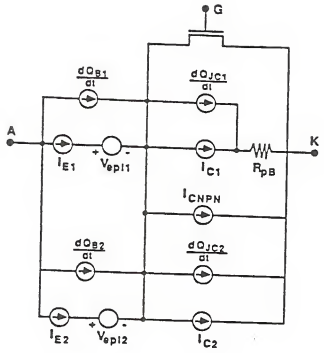

Figure 5-4. Network representation for the LIGBT mode of operation.

anode (Q_1) becomes forward-biased and begins to inject holes into the base region, subsequently modulating R_{epi} and increasing the conductance of the device. Experimental decomposition of the total current into its constituent anode end drain components has revealed that this abrupt increase in conductance, after the LIGBT is activated, results primarily from the modulation of R_{epi} and not from an increase in the anode (BJT) current. The modulation of this resistance tends to increase the DMOST current, but also tends to limit the excitation of Q_1, which is driven by the internal voltage drop. We note that physical insight predicts and experimental results confirm that this drop activates predominantly Q_1 and not Q_2, which is one reason why our assumed partitioning is representative.

In Figure 5-5 we show the experimental decomposition of anode and drain current for the HIGBT mode of operation. Also shown, for comparison, is the LIGBT current-voltage characteristic. Figure 5-5 clearly illustrates that the anode current in the HIGBT mode is only a small fraction of the total current, and furthermore, only a fraction of the IGBT current. This decompostion and comparison of internal currents verifies our partioning scheme and also explains why the latch-up onset for the HIGBT mode is much greater than that for the LIGBT mode. In both modes of operation the emitter current of Q_1, I_{E1}, is approximately the same at the onset of latch-up. Obviously however, the primary

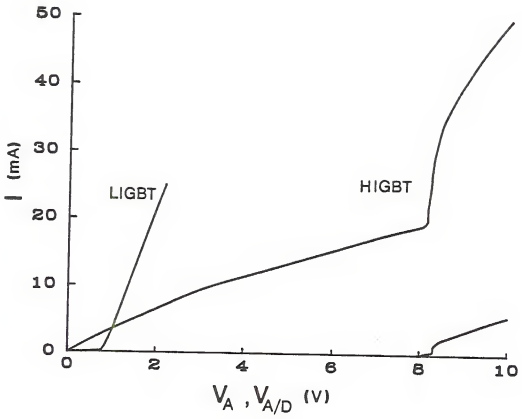

Figure 5-5. Measured LIGBT current versus the anode voltage and measured HIGBT current and anode component of HIGBT current versus the anode/drain (shorted) voltage.

conduction mechanisms and the appropriate partitioning of a particular HIGT depend critically on the device geometry, as shown in [Mu87], and demonstrated in Section 5.4.

The SPICE model for the hybrid device is shown in Figure 5-6. It contains modules for the MOSFET, two resistors R_{nS} and R_{nB}, the sum of which is R_{epi}, and a single lateral pnp transistor, Q_1. The value for R_{nB} (45Ω), which we assume to be constant, is estimated by noting that it takes about 0.6V (a diode drop) of internal voltage drop at the trigger current to turn on Q_1. The modulation of R_{epi} is semi-empirically accounted for in R_{nS} which is simulated by a UDCS, as discussed below.

The portion of the DMOST drain resistance associated with R_{nS} is a function of the total majority carrier concentration, and thus is a function of the carrier injection by Q_1. The variation of R_{nS} with injection level is modeled by using an average excess hole (electron, p=n) density, $\bar{p}$:

$$\bar{p} \triangleq \frac{1}{W}\int_0^W p(x)dx = \frac{Q_{B1}}{qWA} \qquad (5\text{-}10)$$

where p(x) is given by (5-1), and Q_B is given by (5-7). We can use (5-10) to express R_{nS}:

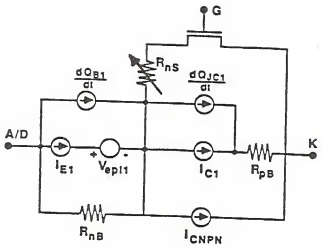

Figure 5-6. Network representation for the HIGBT mode of operation.

$$R_{nS} = \frac{L}{A_V \sigma} = \frac{L}{A_V q \mu_n (N_{epi} + \bar{p})} \qquad (5\text{-}11)$$

where L is the resistor length, A_V is the vertical cross-sectional area, and σ is the conductivity, which depends on $\bar{p}$. A simple algebraic manipulation and substitution for $\bar{p}$ yields:

$$R_{nS} = \frac{R_0}{1 + \frac{Q_{B1}}{qAWN_{epi}}} \quad , \qquad (5\text{-}12)$$

where R_0 is the value of R_{nS} when $\bar{p}$=0.

Both the LIGBT mode and the HIGBT mode can undergo static or dynamic latch-up. Static latch-up occurs when the collector current of Q_1, I_{C1}, produces approximately a diode voltage drop across the lateral resistance R_{pB} in the base of the parasitic n^+pn^- transistor. When this voltage drop develops, electrons are injected by the n^+pn^- BJT into the base of Q_1, increasing its conduction, and hence triggering the regenerative process associated with the SCR [Gh77] defined by Q_1 and the n^+pn^- BJT. Removal of the gate voltage at this point will not turn off the LIGBT or HIGBT since the DMOST supplies only a small fraction of the base current for Q_1, and the main path for current flow is now through the SCR, which can only be turned off by reducing the total current below the holding point.

Experimental results and computer simulations have indicated that the latch-up point is only a weak function of the gate voltage and that the base resistance, R_{pB}, is the most important parameter in determining the onset of latch-up because of the exponential voltage dependence of the injected electrons. We note that the gain of the n^+pn^- BJT also has an influence on the latch-up point, albeit not a strong one. In the dynamic case, both the charging current, $\frac{dQ_{JC}}{dt}$, and the transient collector current contribute to the voltage drop across R_{pB} and hence aid in inducing latch-up.

The onset of latch-up in both the LIGBT and HIGBT modes is simulated by the network models in Figure 5-4 and Figure 5-6 via a voltage-controlled current source I_{CNPN} ($\triangleq I_{SS}\exp(V_{pB}/V_T)$) in which the controlling voltage, V_{pB}, is developed across the assumed constant n^+pn^- base resistance, R_{pB}. The pre-exponential factor, I_{SS}, is related to the gain of the n^+pn^- BJT through the Gummel number. However, PISCES simulations have shown that R_{pB} undergoes significant conductivity modulation just prior to latch-up, and hence R_{pB} and I_{SS} should be considered as semi-empirical modeling parameters. Because of the physical nature of our models, the values used for I_{SS} ($2X10^{-14}$A) and R_{pB} (88Ω) are close to those predicted from PISCES simulations. Note in Figure 5-4 and Figure 5-6 that

the onset of latch-up is properly accounted for in the models as the charging current, $\frac{dQ_{JC1}}{dt}$, contributes to the voltage drop across R_{pB} and hence helps to induce latch-up.

5.4 Simulations/Verification

In Figure 5-7 we show model-simulated and measured current-voltage curves for the LIGBT mode of operation for three different values of the gate voltage. For illustrative clarity, the measured curves were cut off just prior to latch-up. The agreement between experiment and theory is good (~10% error), thus lending support to our particular partitioning and modeling methodology. Discrepancies between the model predictions and experimental results may be attributed to the first-order DMOST model (SPICE/Level 2) that we used.

In Figure 5-8 we compare measured and model-simulated transient turn-off characteristics of the LIGBT. At time t=0 the gate voltage is removed and a typical two-phase turn-off transient, as discussed in Chapter 3, is observed. Our model simulations are in good agreement with experiment. Discrepancies between the model and experiment may be attributed to parasitics associated with the probe station, since our transient measurements were performed on a wafer and not on mounted devices. The turn-off time may seem faster than expected for a lifetime of 2.6μs, but this is due to the large proportion of base current, a

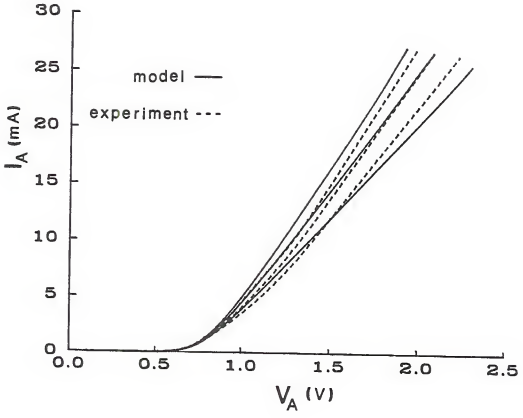

Figure 5-7. Model-simulated (solid) and measured (dashed) LIGBT anode current versus anode voltage for three values of gate voltage (V_g = 12V, 10V and 8V from left to right). The measured curves are terminated just prior to the onset of latch-up; the model-simulated curves are terminated just prior to the predicted latch-up onset.

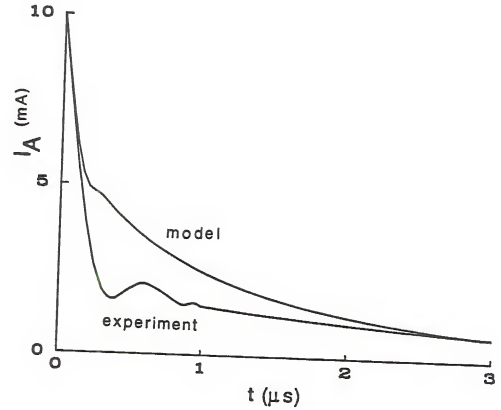

Figure 5-8. Model-simulated and measured LIGBT anode current versus time for a resistive load of 300 Ω and off-state voltage of 4.5 V. The gate voltage of 10 V falls to zero in 200 ns.

substantial fraction (~1/2) of which is p^+-emitter recombination (first term in (5-4)). The expeditious effects of anode recombination on the LIGT turn-off transient have been demonstrated in Chapter 3. We stress that such transient simulations are not possible with conventional SPICE transistor models. We also note that if the gate voltage is removed fast enough, then the sum of the transient collector current and collector-base junction displacement current may be sufficient to forward bias the n^+pn^- transistor and subsequently cause dynamic latch-up. For the circuit conditions shown in Figure 5-8, dynamic latch-up will occur if the gate voltage is removed in less than five nanoseconds.

In Figure 5-9 we show measured current-voltage curves, terminating at latch-up, for the HIGBT mode of operation for three different values of gate voltage. It can be seen that the trigger current for the LIGBT (Q_1) excitation is approximately 13mA, independent of V_G, implying that an internal voltage drop is responsible for the triggering. The onset voltage may be estimated by using our network model for the HIGBT shown in Figure 5-6 and noting that the applied voltage splits between R_{nB}, R_{nS}, and the DMOST channel resistance. The total voltage across the HIGBT, just prior to triggering, consists of three terms: a channel drop, V_{CH}, which depends on the DMOST gate voltage, a drop across R_{nS}, and a drop across R_{nB}, which is

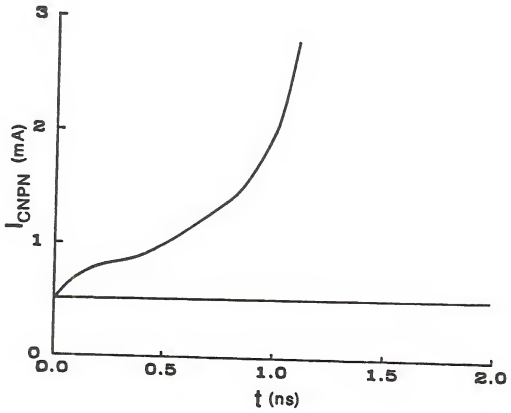

Figure 5-9. Measured HIGBT anode/drain current versus anode/drain voltage for three values of gate voltage (V_g = 6V, 8V and 10V from right to left respectively). The measured curves are terminated just prior to the onset of latch-up.

approximately a diode drop, V_d. The voltage drop across R_{nS} then is simply the current through R_{nB} times R_{nS} ($V_d \cdot R_{nS}/R_{nB}$). The total voltage across the HIGBT, just prior to triggering, may then be expressed as, $V_{CH}+V_d(1+R_{nS}/R_{nB})$. Thus the relative magnitudes of R_{nS} and R_{nB} greatly influence the onset voltage. To effect optimal HIGBT design (low onset voltage), R_{nS} should be made much less than R_{nB}. Later we will show that R_{nB} plays an important role in determining the transient turn-off characteristics. The increase in total current immediatly after the triggering is due predominantly to an increase in the DMOST current as a result of modulating R_{nS} and as discussed previously in Section 5.3.

In Figure 5-10 we show corresponding SPICE model current-voltage curves for the HIGBT. Note that the triggering points for the hybrid mode of operation are reliably predicted, as well as the latch-up onsets. We note, however, that although our model modestly simulates the DMOST region, the predicted conductance in the hybrid mode is less accurate. This inaccuracy is due in part to the semi-empirical approximate representation (5-11) of the modulated DMOST resistance. More physical UDCS modeling of this highly nonlinear modulation could be done to improve the accuracy. However, to effect a generally valid model, a more physical DMOST module should be developed to replace the simple SPICE/Level 2 model.

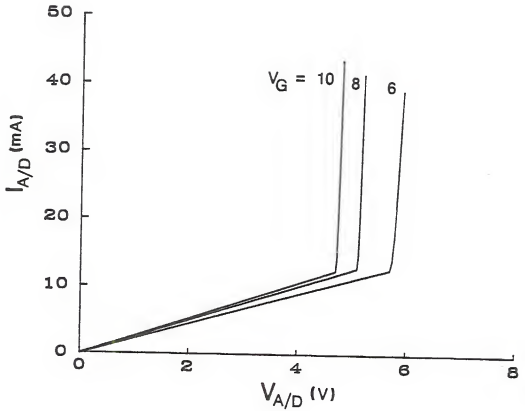

Figure 5-10. Model-simulated HIGBT anode/drain current versus anode/drain voltage for three values of gate voltage (V_g =10V, 8V and 6V). The model-simulated curves are terminated just prior to the model-predicted latch-up onset.

In Figure 5-11 we show a model-simulated transient turn-off characteristic for the HIGBT. Because the HIGBT current for our test structure consists mainly of DMOST drain current, the magnitude of the first phase is quite large, but the conventional two-phase IGBT turn-off transient is clearly manifested. However, the influence of R_{nB}, which provides a path for carrier removal during the transient, needs to be physically characterized so that design criteria for an optimal HIGBT structure may be suggested [Fo87]. A cursory analysis of how R_{nB} affects the HIGBT transient turn-off is presented below.

To develop physical insight into how R_{nB} affects transient response, we extend the analysis in Chapter 2 by adding a term (V_{JEB}/R_{nB}) to equation (2-15), thus accounting for carrier removal through the drain during phase two. If we neglect all components of recombination current, assuming the dominant component of current is carrier removal through R_{nB}, then the following simple differential equation for the charge residing in the base region during phase two results:

$$\frac{dQ_B}{dt} = - \frac{V_{JEB}}{R_{nB}} \quad . \qquad (5\text{-}13)$$

If one assumes that V_{JEB} remains relatively constant ($\approx V_d$)

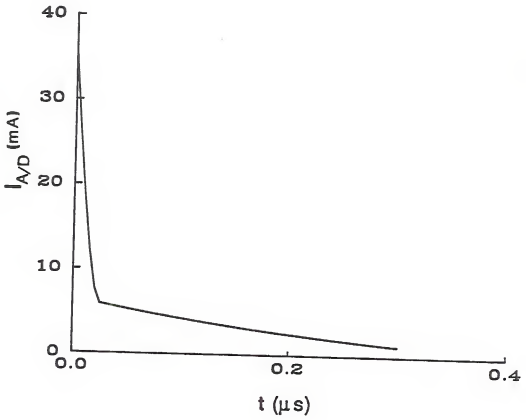

Figure 5-11. Model-simulated HIGBT anode/drain current versus time for a resistive load of 100 Ω and off-state voltage of 6 V. The gate voltage of 10 V falls to zero in 25 ns.

during phase two, then the solution to (5-12) implies a fast linearly decaying current, inversly proportional to R_{nB}. Our model simulations for the HIGBT turn-off transient (Figure 5-11) clearly show the predicted linear nature of the second phase. Experimental corroboration of this analysis can be inferred from [Go86], where the decay during phase two is found to be approximately linear in time. Thus, to effect a fast turn-off, R_{nB} should be made as small as possible, but consistent with the constraint for a low onset voltage ($R_{nS}<<R_{nB}$).

The circuit topology as depicted in Figure 5-4, and used in our simulations, is not capable of maintaining a latched state (steady-state solution) during transient operations in SPICE. As a consequence, it is not possible to observe dynamic latch-up directly, i.e., to see the anode current remain constant with time when the gate voltage is removed. However, the onset of dynamic latch-up may be indirectly observed by monitoring the current I_{CNPN}, which represents the injection of electrons by the parasitic n^+pn^- BJT.

We demonstrate the ability of the modeling methodology to predict the onset of dynamic latch-up in Figure 5-12, where we have plotted the current, I_{CNPN}, as a function of time for a resistively loaded LIGBT turn-off transient. The sharp increase in I_{CNPN} during the fast turn-off transient (T_{Fall}=2ns) indicates the onset of dynamic latch-up and is consistent with

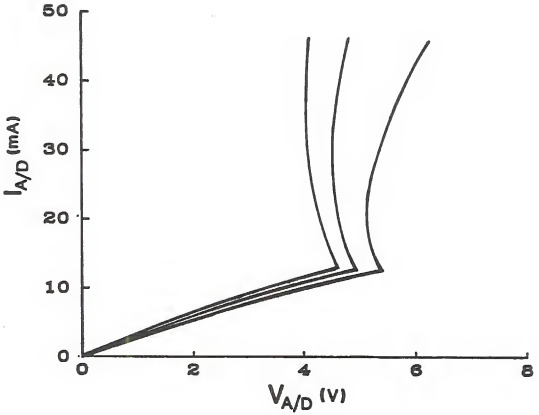

Figure 5-12. Model-simulated I_{CNPN} current versus time for a resistive load of 125 Ω and off-state voltage of 5 V. The gate voltage (10V) has a fall time (T_{Fall}) of 2 ns for the upper curve and a T_{Fall} of 200 ns for the lower one.

experimental results. Note that for a slower turn-off transient (T_{Fall}=200ns), I_{CNPN} remains unchanged during the time period shown in Figure 5-12. Eventually, for such a slow transient, I_{CNPN} will decrease to zero and the onset of dynamic latch-up will not manifest itself. Our simulations indicate that the primary current responsible for initiating the onset of dynamic latch-up for the above circuit conditions is the displacement current, $\frac{dQ_{JC1}}{dt}$. However, for other circuit conditions the increase in the transient collector current could be made significant. We note that the utility of the model to predict the onset of dynamic latch-up will make it useful for optimizing device design under an actual circuit (transient) environment.

5.5 Summary

We have developed a device modeling methodology needed for the CAD of HV/P ICs that is also useful for optimal device (process) design. The methodology is based on a regional partitioning of LIGBT structures through physical insight gained from numerical simulations (PISCES) and experimental results (special test devices). The regional partitioning of a lateral structure defines an array of new one-dimensional device modules, which properly (physically) model the unique features of HV/P devices. We have demonstrated this flexible quasi-2-D methodology on an LIGBT test structure for all possible active modes of

operation. Both dc and transient measurements, including static and dynamic latch-up, support the modeling methodolgy. In addition, this study points out the need for further work in extending previous DMOST models [Su80] for cases when the enhancement-mode device has its bulk region conductivity-modulated, as is the case for the LIGBT. Also, the physics underlying the onset of latch-up needs clarification, especially in regards to the conductivity modulation of R_{pB} prior to latch-up.

The constituent charge-based modules, which are easily implemented into SPICE via UDCSs, allow for a network representation of the structure that can be used to simulate the device under actual circuit (transient) conditions, a feature most device simulators do not have. Consequently, the methodology may be useful in optimizing device design under an actual transient environment, in addition to the CAD capability it affords.

CHAPTER 6
SUMMARY AND CONCLUSIONS WITH RECOMMENDATIONS

6.1 Summary and Conclusions

The culmination of this dissertation manifests itself in Chapter 5 where we brought together the physical insights and techniques presented in earlier chapters to develop a methodology for constructing, and implementing in SPICE, physical network representations for a general class of HV/P IC devices exemplified by the LIGBT. We verified our network models by comparison with PISCES simulations and by comparison with experimental results obtained from specially designed test structures. Included in the novel network representations were several high-injection and unique effects inherent in HV/P IC devices, heretofore not represented in more empirical (less accurate) equivalent circuit models. The effects characterized included conductivity modulation, enhanced back injection, multidimensional current flow, and the onset of static and dynamic latch-up.

In Chapter 2 we presented a general methodology for modeling lateral ($p^+pn^-n^+$) structures used in HVICs. The model, verified by direct comparison with experimental results obtained from specially designed test structures, was useful in extending the methodology presented in Chapters 4 and 5 to include the effects of the punch-through shield (buffer region) on the carrier transport in LIGBT structures. The physical insight gained in developing a GDS model was later used in Chapters 4 and 5 to develop models for IGBT structures, in particular with regard to the proper accounting for the PIN-diode physics, which underlies the IGBT operation.

In Chapter 3 a physical , quasi-two-dimensional analytical model for the IGBT turn-off transient was developed. The utility of the physical insight gained from the model was instrumental in suggesting optimal device and structural parameter values for decreasing the turn-off time without significant derogation of the on-state current handling capability. In addition, the phenomenological insight afforded by the model allowed for the identification of the significant charging mechanisms controlling the transient response, and thus permitted key simplifications to be made in the development of the network models presented in Chapters 4 and 5.

In Chapter 4 we presented an initial endeavor at devoloping a methodology for modeling an IGBT structure and for implementing the model in SPICE via UDCSs. The

methodology presented was flexible and enabled for the first time the simulation of the unique effects of conductivity modulation, latch-up (static and dynamic), and moving boundary conditions; however, it required recourse to FORTRAN subroutines for the solution of the implicit nonlinear equations rather than utilizing the nonlinear equation solver inherent in the SPICE2 source code. Thus, CPU times required for simulations using the methodology were considerably longer than those using invalid built-in SPICE2 models; however, they are not prohibitive for small-scale circuits, where one or two HV/P IC devices are used. The preliminary work in Chapter 4 provided the impetus for developing a more effecient means of problem formulation and subsequent SPICE2 implementation for HV/P IC device models. Chapter 5, as discussed above, extended and refined the work presented in Chapter 4.

6.2 Recommendations

There are several avenues for further research which would enhance the acceptance of our modeling methodology. For a complete HV/P IC CAD facility, a library of HP/V device modules is essential. Ideally, such a library would include a number of internal SPICE2 HV/P device modules, consisting of, but not limited to models for the PIN-diode, the DMOST, the LIGBT, and the wide-base BJT. Using our methodology, a user could then construct his own model

(subcircuit) for a particular HV/P structure, without recourse to UDCSs. We now outline several research areas essential for the construction of a CAD library for HV/P IC design.

First, we recommend the extension of our empirical DMOST model. Since the DMOST is an integral part of many HV/P devices, it is essential that a simple and accurate model for this common HV/P device be developed. The device physics underlying the DMOST when the drain region becomes conductivity modulated needs clarification. The simple Sun and Plummer [Su78] model is not applicable to DMOSTs in which the drain undergoes significant conductivity-modulation, as in the LIGBT.

Second, we recommend extending our wide-base BJT model (Appendix A) for all regions of operation, thus making it a viable circuit-simulation tool. In addition, since nearly all LIGBTs employ punch-through shields, a more representative wide-base BJT would be a $p^+n^+n^-p$ structure. The insights gained from modeling the GDS in Chapter 2 would be helpful in characterizing such a transistor structure.

Third, we recommend the creation of a standard PIN-diode model for circuit simulation. Many HV/P structures contain this basic device, and such a model would be useful for parameter-extraction methods involving optimization techniques, as was done in Chapter 5.

Fourth, we recommend extending our first-order latch-up model used in the LIGBT network representation. The physics underlying the latch-up process, including the latch current and the holding current, needs clarification.

Fifth, we recommend the incorporation of all device models into the SPICE code, as we feel that UDCSs are primarily a means for model development. The inherent problems of nonstandard coding, nonuniform convergence criteria, numerical instabilites, and long CPU times preclude the use of UDCSs for practical circuit simulation in an industrial environment. For example, the eleven UDCSs comprising the LIGBT model in Chapter 5 contain nearly 1500 lines of FORTRAN code (see Appendix B). If the model were directly implemented into the SPICE code, only a few dozen lines would be needed. Thus, for universal acceptance of our modeling methodology, the direct incorporation of our models into the SPICE code is of paramount importance.

APPENDIX A
HIGH-CURRENT TRANSPORT IN WIDE-BASE BJTs

In this appendix we briefly overview carrier transport in wide-base (p^+n^-p and n^+p^-n) BJT structures. The approach is based on an ambipolar transport analysis and has its historical roots set in PIN-diode theory [He68].

Consider a p^+n^-p transistor structure operating in the forward-active mode for which high injection ($p=n>>N_D$) obtains in the n^- base region. A straightforward ambipolar analysis [He68] can be used to equate the electron recombination current density in the p^+ emitter, J_N, to the electron current density in the n^- base at the edge (x=0) of the emitter-base junction space-charge region (neglecting any space-charge region recombination), thereby yielding the following relation between J_N and the total emitter current density, J_E:

$$J_N = \frac{b}{b+1} J_E + qD_A \frac{dp}{dx}\bigg|_{x=0} \qquad (A-1)$$

where D_A is the ambipolar diffusivity, dp/dx is the gradient of the hole (electron) concentration. For increasing current densities, the second term on the right-hand side of A-1 will always become negligible because it is proportional to p(0) (p(x): x=0), whereas J_N is proportional to $p(0)^2$ [Gh77]. Thus, at high current densities the base current consists primarily of emitter recombination current, as shown in Chapter 2, and equation A-1 can be used to to find a limiting value for the BJT current gain:

$$\beta_{pnp} = \frac{J_E - J_N}{J_N} \simeq \frac{1}{b} . \qquad (A-2)$$

A similar analysis for an n^+p^-n structure yields a different high current limit for the gain:

$$\beta_{npn} \simeq b . \qquad (A-3)$$

Physically, the difference between the high-current βs for pnp and npn transistors results from the unequal electron and hole mobilities. Thus typical npn and pnp BJTs used in HV/P ICs have very different limiting βs. If

carrier-carrier scattering effects [Gh77] are taken into account, the mobility ratio reduces to about two, therefore the limiting βs will differ roughly by a factor of four. The physical insight afforded by this simple analysis can be used to explain several of the fundamental differences between n- and p-channel IGBTs, such as the lower latch-up onset for p-channel IGBTs.

The details for a rudimentary, first-order, high-current transport model for a wide-base BJT have been described in chapters 4 and 5 and have been summarized, pictorially, in Figure 5-2. Needed additions to that high-current model would include modifications to the system of implicit model equations to account for the effects of quasi-saturation [Je87] and carrier mobility reduction due to carrier-carrier scattering [Gh77] (refer to Chapter 2).

APPENDIX B
UDCS/SLICE/SPICE MODEL IMPLEMENTATION

In this appendix we briefly overview a representative UDCS SLICE/SPICE implementation of a charge-based network representation for a wide-base, low-β pnp BJT, as depicted in Figure 5-2.

The general theory and mechanical details behind the implementation of steady-state UDCS network models into SLICE/SPICE can be found in the SLICE Manual Rev. 4.08 [Ha84]. The general theory behind the implementation of transient UDCS network models in SLICE is discussed in Veeraraghavan et al. [Ve86].

The implicit nature of the network model and the novel use of numerical derivatives (finite differences) for the transconductances and transcapacitances are delineated via comment statements in the following FORTRAN code listing, which details each UDCS subroutine for the BJT model shown in Figure 5-2.

```
C
C*****************************************************************
C THE FOLLOWING LISTING IS A SUBROUTINE WHICH CALCULATES
C THE EMITTER CURRENT, IE, GIVEN THE NODE VOLTAGES VBE AND VBC
C THE SLICE USERS MANUAL SHOULD BE CONSULTED FOR THE SPECIAL
C FORMAT USED IN CIRCUIT FILES FOR UDCS DEFINED ELEMENTS
C*****************************************************************
C
      SUBROUTINE UIELT1(Y,IFLAG,LP,NP,LC,NC,JERROR)
      IMPLICIT DOUBLE PRECISION (A-H,O-Z)
      DOUBLE PRECISION ND,NI,JN0,IE1,LA
      SPECIAL COMMON BLANK
      COMMON/BLANK/X(64)
      GOTO(50,100,200,300),IFLAG+2
50    CONTINUE
        IF(NC.NE.2) JERROR = -99010
      GOTO 99910
100   CONTINUE
      PHI=.6
      ES=1.035E-12
      NI=1.3E10
      UN=1350.0
      UP=480.0
       B=UN/UP
       Q=1.6E-19
       VT=.02586
       DA=2*VT*UN*UP/(UN+UP)
      WB=    X(LP+1)
      T0=    X(LP+2)
      JN0=   X(LP+3)
      ND=    X(LP+4)
      AE1=   X(LP+5)
        H=   X(LP+6)
       CF=   X(LP+7)
      XX2=   X(LP+8)
      XX3=   X(LP+9)
      VBE=   X(LC+1)
      VBC=   X(LC+2)
       TH=2*T0
       LA=SQRT(DA*TH)
C
C SET Y = VALUE OF IE1
C

C
C  CONVERGENCE ENHANCEMENT
C
      IF(VBE.GT.0.80)THEN


       VBE=CF*VT*LOG(VBE/VT)
       END IF
     IF(VBE.LT.0.55)THEN
       P0=NI**2*EXP(VBE/VT)/ND
       Y = Q*AE1*DA/WB*P0
       FLGY = 0.0
       GOTO 987
       END IF
     IF((VBE.GT.0.55).AND.(VBE.LT.0.80))
       P0=NI**2/ND*EXP(VBE/VT)
     END IF
     FLGY=2.0
C
C
      W = WB -(2*ES*(PHI+ABS(VBC))/(ND*Q))**.5
      Y  = (B+1)/B*(AE1*JN0*P0**2/NI**2+Q*DA*AE1*P0/LA/TANH(H/LA))
C
987   CONTINUE
      GOTO 99910
200   CONTINUE
```

```
C SET Y = VALUE OF DIE1/DVBE
C
      IF(FLGY.LT.1.0)THEN
         Y = Q*AE1*DA/WB*P0/VT
      GOTO 876
      END IF
      Z1 = 2*(B+1)/B*AE1*JN0*P0**2/N1**2/VT
      Z2 = (B+1)/B*Q*DA*AE1*P0/LA/VT/TANH(W/LA)
      Y = Z1 + Z2
876   CONTINUE
       GOTO 99910
300    CONTINUE
C
C SET Y = VALUE OF DIE1/DVBC BY FINITE DIFFERENCE
C
      IF(FLGY.LT.1.0)THEN
      Y=0.0
      GOTO 765
      END IF
       W = WB -(2*ES*(PHI+ABS(VBC))/(ND*Q))**.5
       Y1 = (B+1)/B*(AE1*JN0*P0**2/N1**2+Q*DA*AE1*P0/LA/TANH(W/LA))
       VBC = VBC + H
       W = WB -(2*ES*(PHI+ABS(VBC))/(ND*Q))**.5
       Y2 = (B+1)/B*(AE1*JN0*P0**2/N1**2+Q*DA*AE1*P0/LA/TANH(W/LA))
       Y =(Y2-Y1)/H
       VBC=VBC-H
          GOTO 99910

  765    CONTINUE
  99910 CONTINUE
        RETURN
        END

  C
  C*******************************************************
  C THE FOLLOWING LISTING IS A SUBROUTINE WHICH CALCULATES
  C THE COLLECTOR CURRENT, IC, GIVEN THE NODE VOLTAGES VBE
  C AND VBC THE SLICE USERS MANUAL SHOULD BE CONSULTED FOR
  C THE SPECIAL FORMAT USED IN UDCS IMPLEMENTATION
  C *******************************************************
  C
        SUBROUTINE UICLT1(Y,IFLAG,LP,NP,LC,NC,JERROR)
        IMPLICIT DOUBLE PRECISION (A-H,O-Z)
        DOUBLE PRECISION ND,NI,JN0,IC1,LA
        SPECIAL COMMON BLANK
        COMMON/BLANK/X(64)
        GOTO(50,100,200,300),IFLAG+2
  50    CONTINUE
           IF(NC.NE.2) JERROR = -99010
        GOTO 99910
  100   CONTINUE
        PHI=.6
        ES=1.035E-12
        NI=1.3E10
        UN=1350.0
        UP=480.0
         B=UN/UP
         Q=1.6E-19
         VT=.02586
         DA=2*VT*UN*UP/(UN+UP)
  C
  C SET Y = VALUE OF IC1
  C
        WB=    X(LP+1)
        T0=    X(LP+2)
        JN0=   X(LP+3)
        ND=    X(LP+4)
        AE1=   X(LP+5)
          H=   X(LP+6)
```

```
      XX1=   X(LP+7)
      XX2=   X(LP+8)
      XX3=   X(LP+9)
      VBE=   X(LC+1)
      VBC=   X(LC+2)
       TH=2*T0
       LA=SQRT(DA*TH)

C
C  CONVERGENCE ENHANCEMENT
C
      IF(VBE.GT.0.80)THEN
        VBE=VT*LOG(VBE/VT)
       END IF
      IF(VBE.LT.0.55)THEN
        P0=NI**2*EXP(VBE/VT)/ND
        FLGY=0.0
        Y = Q*AE1*DA*P0/WB
        GOTO 987
      END IF
      IF((VBE.GT.0.55).AND.(VBE.LT.0.80))
        P0=NI**2/ND*EXP(VBE/VT)
      END IF
        FLGY=2.0
C
C
      W = WB -(2*ES*(PHI+ABS(VBC))/(ND*Q))**.5
      S1= AE1*JN0/B*(P0/NI)**2
      S2= Q*AE1*DA*P0*(COSH(W/LA)+B)/LA/SINH(W/LA)/B
      Y  = S1 + S2
C
987   CONTINUE
      GOTO 99910
200   CONTINUE
C
C SET Y = VALUE OF DIC1/DVBE
C
      IF(FLGY.LT.1.0)THEN
        Y = Q*AE1*DA*P0/WB/VT
       GOTO 876
      END IF
      Z1 = 2*AE1/B/VT*JN0*(P0/NI)**2
      Z2 = AE1*Q*DA*P0*(COSH(W/LA)+B)/LA/SINH(W/LA)/VT/B
      Y = Z1 + Z2
876   CONTINUE
       GOTO 99910
300    CONTINUE
C


 C
 C SET Y = VALUE OF DIC1/DVBC
 C
       IF(FLGY.LT.1.0)THEN
        Y = 0.0
        GOTO 765
       END IF
       W = WB -(2*ES*(PHI+ABS(VBC))/(ND*Q))**.5
       Y1= Q*AE1*DA*P0*(COSH(W/LA)+B)/LA/SINH(W/LA)/B
         VBC= VBC + H
       W = WB -(2*ES*(PHI+ABS(VBC))/(ND*Q))**.5
       Y2= Q*AE1*DA*P0*(COSH(W/LA)+B)/LA/SINH(W/LA)/B
       Y = (Y2-Y1)/H
       VBC = VBC-H
765    CONTINUE
          GOTO 99910
99910 CONTINUE
      RETURN
      END
```

```
C*************************************************
C  THIS SUBROUTINE CALCULATES THE VOLTAGE DROP DUE
C TO CONDUCTIVITY MODULATION IN THE BASE REGION
C AS A FUNCTION OF THE NODE VOLTAGES VBE AND VBC
C THE SLICE USERS MANUAL SHOULD BE CONSULTED FOR
C DETAILS IN USING THIS SUBROUTINE IN A UDCS CIRCUIT
C FILE
C*************************************************
      SUBROUTINE UVEPT1(Y,IFLAG,LP,NP,LC,NC,JERROR)
      IMPLICIT DOUBLE PRECISION (A-H,O-Z)
      DOUBLE PRECISION ND,NI,JNO,IE1,LA
      $PECIAL COMMON BLANK
      COMMON/BLANK/X(64)
      GOTO(50,100,200,300),IFLAG+2
50    CONTINUE
        IF(NC.NE.2) JERROR = -99010
      GOTO 99910
100   CONTINUE
      PHI=.6
      ES=1.035E-12
      NI=1.3E10
      UN=1350.0
      UP=480.0

      B=UN/UP
      VT=.025B6
      Q=1.6E-19
      DA = 2*VT*UN*UP/(UN+UP)
C
      WB=X(LP+1)
      TO=  X(LP+2)
      JNO = X(LP+3)
      ND=X(LP+4)
      AE1 = X(LP+5)
      H = X(LP+6)
      XX1=X(LP+7)
      XX2=X(LP+B)
      XX3=X(LP+9)
      VBE= X(LC+1)
      VBC= X(LC+2)
      TH=2*TO
       LA = SQRT(DA*TH)
C
C CONVERGENCE ENHANCEMENT
C
          IF(VBE.GT.0.80)THEN
            VBE=VT*LOG(VBE/VT)
            END IF
          IF(VBE.LT.0.55)THEN
            FLGY = 0.0
            P0=NI**2*EXP(VBE/VT)/ND
            Y = 0.0
            GOTO 987
          END IF
          IF((VBE.GT.0.55).AND.(VBE.LT.0.80))
           P0=NI**2/ND*EXP(VBE/VT)
           END IF
            FLGY = 2.0
C
C CALCULATE W THE ACTIVE BASE WIDTH AND
C CALCULATE XS, THE POINT AT WHICH P(X)=ND
C
         W= WB - (2*ES*(PHI+ABS(VBC))/(ND*Q))**.5
         ZZ= ND/P0*SINH(W/LA)
         XS=W-LA*LOG(ZZ + SQRT(ZZ**2+1))
C
C SET Y = VALUE OF VEP1
C
          IE1=(B+1)/B*(AE1*JNO*P0**2/NI**2+Q*DA*AE1*P0/LA/TANH(W/LA))
          VDEM=VT*(B-1)/(B+1)*LOG(P0/ND)
          VEP1=VDEM-SINH(W/LA)*IE1*LA/AE1/Q/(UN+UP)/P0*
       &LOG(TANH((W-XB)/LA)/TANH(W/LA))
```

```
        Y = VEPI
987     CONTINUE
        GOTO 99910
200     CONTINUE
C
C SET Y = VALUE OF DVEP/DVBE
C
       IF(FLGY.LT.1.0)THEN
        Y = 0.0
        GOTO 876
       END IF
         IFLG=1
567     CONTINUE
C
C CALCULATE W THE ACTIVE BASE WIDTH AND
C CALCULATE XS, THE POINT AT WHICH P(X)=ND
C
         W= WB - (2*ES*(PHI+ABS(VBC))/(ND*Q))**.5
         ZZ= ND/P0*SINH(W/LA)
         XS=W-LA*LOG(ZZ + SQRT(ZZ**2+1))
C
C SET Z = VALUE OF VEPI
C
         IE1=(B+1)/B*(AE1*JNO*P0**2/NI**2+Q*DA*AE1*P0/LA/TANH(W/LA))
         VDEM=VT*(B-1)/(B+1)*LOG(P0/ND)
         VEPI=VDEM-SINH(W/LA)*IE1*LA/AE1/Q/(UN+UP)/P0*
     &LOG((TANH((W-XS)/LA)/TANH(W/LA))
         Z2=VEPI
            IF(IFLG.EQ.1)THEN
               Z1=VEPI
               VBE=VBE+H
               IFLG=2
               GOTO 567
            END IF
          VBE=VBE-H
          Y=(Z2-Z1)/H
876     CONTINUE
        GOTO 99910
300     CONTINUE
C
C SET Y = VALUE OF DVEP/DVBC
C
       IF(FLGY.LT.1.0)THEN
        Y = 0.0
        GOTO 765
       END IF
         IFLG=1
789     CONTINUE


C
C CALCULATE W THE ACTIVE BASE WIDTH AND
C CALCULATE XS, THE POINT AT WHICH P(X)=ND
C
         W= WB - (2*ES*(PHI+ABS(VBC))/(ND*Q))**.5
         ZZ= ND/P0*SINH(W/LA)
         XS=W-LA*LOG(ZZ + SQRT(ZZ**2+1))
C
C SET Z = VALUE OF VEPI
C
```

```
          IE1=(B+1)/B*(AE1*JN0*P0**2/NI**2+Q*DA*AE1*P0/LA/TANH(W/LA))
          VDEH=VT*(B-1)/(B+1)*LOG(P0/ND)
          VEPI=VDEM-SINH(W/LA)*IE1*LA/AE1/Q/(UN+UP)/P0*
     &LOG(TANH((W-XS)/LA)/TANH(W/LA))
          Z2=VEPI
            IF(IFLG.EQ.1)THEN
                Z1=VEPI
                VBC=VBC+H
                IFLG=2
                GOTO 789
              END IF
           VBC=VBC-H
           Y=(Z2-Z1)/H
765        CONTINUE
           GOTO 99910
99910   CONTINUE
        RETURN
        END

C*************************************************
C THIS SUBROUTINE CALCULATES THE CHARGE IN THE BASE
C REGION AS A FUCTION OF THE NODE VOLTAGES VBE AND VBC
C FOR THE CHARACTERIZATION OF THE TRANSIENT CHARGING
C CURRENTS BY A UDCS [VEB6]
C*************************************************
C
        SUBROUTINE UQB1(Y,IFLAG,LP,NP,LC,NC,JERROR)
        IMPLICIT DOUBLE PRECISION (A-H,O-Z)
        DOUBLE PRECISION ND, JN0,NI,JN01
        SPECIAL COMMON BLANK
        COMMON/BLANK/X(64)
        COMMON/STATUS/OMEGA,TIME,DELTA,DELOLD(7),AG(7),VT,XNI,
     & EGFET,MODE,MODEDC,ICALC,INITF,METHOD,IORD,MAXORD,NONCON,
     & ITERNO,ITEHNO,NOSOLV
        COMMON/KNSTNT/TWOPI,XLOG2,XLOG10,ROOT2,RAD,BOLTZ,CHARGE,
     & CTOK,GMIN,RELTOL,ABSTOL,VNTOL,TRTOL,CHGTOL,EPS0,EPSSIL,EPSOX
        IF(TIME.EQ.0.0) THEN
           WB1=X(LP+1)
           T0= X(LP+2)
           JN01=X(LP+3)
           ND=X(LP+4)
           AE1=X(LP+5)
           H=X(LP+6)

           WB=WB1
           JN0=JN01
            A = AE1
        ENDIF
        VT=.02586
        NI=1.3E10
        UN=1350
        UP=480
        B=UN/UP
        PHI=.6
        ES=1.035E-12
        Q=1.6E-19
        DA=2*VT*UN*UP/(UN+UP)
        TH=2*T0
        LA=SQRT(DA*TH)
        GOTO(50,100,200,300),IFLAG+2
 50     CONTINUE
        RETURN
 100    CONTINUE
```

```
C
C   INITIALIZE THE VOLTAGES AND MAKE CURRENT = 0.0 IN DC CASE
C
        VBE= X(LC+1)
        VBC= X(LC+2)
      IF(TIME.EQ.0.0)THEN
          IF(VBE.LT.0.56)THEN
            PO = NI**2/ND*EXP(VBE/VT)
            Y = 0.0
            FLGY=0.0
            GOTO 987
          END IF
          FLGY = 2.0
          IF(VBE.GT.0.78)PO=3E16
          IF((VBE.GT.0.56).AND.(VBE.LT.0.78))
            PO=NI**2/ND*EXP(VBE/VT)
          END IF
      W=WB-(2*ES*(PHI+ABS(VBC))/(ND*Q))**.5
      QB1=Q*A*LA*PO*(COSH(W/LA)-1.0)/SINH(W/LA)
        X(LP+8)= QB1
        Y=0.0
        X(LP+9)=Y
        X(LP+10)=DELTA
        X(LP+11)= QB1
        X(LP+12)=Y
        RETURN
      ELSE
C
C  UPDATE CHARGE AND CURRENT IF LOCAL TRUNCATION ERROR CRITERIA ARE MET

C
          IF((INITF.EQ.6).AND.(DELTA.GE.X(LP+10)))THEN
               X(LP+8)=X(LP+11)
               X(LP+9)=X(LP+12)
          ENDIF
        QB1=Q*A*LA*PO*(COSH(W/LA)-1.0)/SINH(W/LA)
        X(LP+11)=QB1
        X(LP+10)=DELTA
          IF(DELTA.EQ.0.0)THEN
               Y=0.0
          ELSE
               Y=((QB1-X(LP+8))*2.0/DELTA)-X(LP+9)
          ENDIF
        X(LP+12)=Y
      ENDIF
C  NO ERROR CHECKING
       YNDER = 0
987    CONTINUE
       RETURN
200    CONTINUE
C
C SET Y = VALUE OF DQB/DVBE
C
          IF(FLGY.LT.1.0)THEN
               Y = 0.0
               GOTO 876
          END IF
          IF(DELTA.EQ.0.0)THEN
               Y=0.0
          ELSE
     Y =Q*A*LA*PO*(COSH(W/LA)-1.0)/SINH(W/LA)/VT
               Y= 2.0*Y/DELTA
          ENDIF
876    CONTINUE
       RETURN
300    CONTINUE
C
```

```
C
C SET Y = VALUE OF DQB/DVBC
C
            IF(FLGY.LT.1.0)THEN
                 Y = 0.0
                 GOTO 765
            END IF
            IF(DELTA.EQ.0.0)THEN
                 Y=0.0
            ELSE
           Y=Q*A*P0*ES/ND/Q/(2*ES*(PHI+ABS(VBC))/ND*Q)**.5
                 Y= 2.0*Y/DELTA


              ENDIF
  765       CONTINUE
           RETURN
        END


  C*************************************************************
  C THIS SUBROUTINE CALCULATES THE CHARGE ASSOCIATED
  C WITH THE REVERSE-BIASED COLLECTOR-BASE JUNCTION AS A
  C FUNCTION OF THE NODE VOLTAGES VBE AND VBC FOR
  C CHARACTERIZATION OF THE TRANSIENT CHARGING CURRENTS
  C BY A UDCS [VE86]
  C
  C*************************************************************
        SUBROUTINE UDJC1(Y,IFLAG,LP,NP,LC,NC,JERROR)
        IMPLICIT DOUBLE PRECISION (A-H,O-Z)
        DOUBLE PRECISION ND
        SPECIAL COMMON BLANK
        COMMON/BLANK/X(64)
        COMMON/STATUS/OMEGA,TIME,DELTA,DELOLD(7),AG(7),VT,XNI,
       & EGFET,MODE,MODEDC,ICALC,INITF,METHOD,IORD,MAXORD,NONCON,
       & ITERND,ITEMNO,NOSOLV
        COMMON/KNSTNT/TWOPI,XLOG2,XLOG10,ROOT2,RAD,BOLTZ,CHARGE,
       & CTOK,GMIN,RELTOL,ABSTOL,VNTOL,TRTOL,CHGTOL,EPS0,EPSSIL,EPSOX
        IF(TIME.EQ.0.0) THEN
           AC= X(LP+1)
           ND= X(LP+2)
           X1 =X(LP+3)
           X2= X(LP+4)
           X3=X(LP+5)
        ENDIF
        GOTO(50,100,200),IFLAG+2
  50    CONTINUE
        RETURN
  100   CONTINUE
  C
  C   INITIALIZE THE VOLTAGES AND MAKE CURRENT = 0.0 IN DC CASE
  C
          VBC= X(LC+1)
        IF(TIME.EQ.0.0)THEN
          QJC=AC*(2.07E-12*1.6E-19*ND*ABS(.6+VBC))**.5
          QJC=Y
          X(LP+8)= QJC
          Y=0.0
          X(LP+9)=Y
          X(LP+10)=DELTA
          X(LP+11)= QJC
          X(LP+12)=Y
          RETURN
        ELSE
  C
  C  UPDATE CHARGE AND CURRENT IF LOCAL TRUNCATION ERROR CRITERIA ARE MET
  C
                IF((INITF.EQ.6).AND.(DELTA.GE.X(LP+10)))THEN
```

```
                X(LP+8)=X(LP+11)
                X(LP+9)=X(LP+12)
            ENDIF
        QJC=AC*(2.07E-12*1.6E-19*ND*ABS(.6*VBC))**.5
        QJC=Y
        X(LP+11)=QJC
        X(LP+10)=DELTA
            IF(DELTA.EQ.0.0)THEN
                Y=0.0
            ELSE
                Y=((QJC-X(LP+8))*2.0/DELTA)-X(LP+9)
            ENDIF
        X(LP+12)=Y
      ENDIF
C  NO ERROR CHECKING
      YNDER = 0
      RETURN
200   CONTINUE
C
C SET Y = VALUE OF DQJC/DVBC
C
            IF(DELTA.EQ.0.0)THEN
                Y=0.0
            ELSE
                Y= AC*.5*(2.07E-12*1.6E-19*ND)*(ABS(.6*VBC)**-.5)
                Y= 2*Y/DELTA
                Y=0.0
            ENDIF
      RETURN
      END
```

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